



Gowin I2C to ELVDS IP

User Guide

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1 About This Guide

1.1 Purpose

Gowin I2C to ELVDS IP User Guide includes function introductions, signal definitions, functional descriptions, and interface configuration. It can help you quickly learn the features and usage of Gowin I2C to ELVDS IP.

1.2 Related Documents

The latest user guides are available on our Website. You can find the related documents at www.gowinsemi.com.

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
I ² C	Inter-Integrated Circuit

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

I²C (Inter-Integrated Circuit) is a kind of two-wire serial bus that is used to connect the micro-controller with its peripherals.

Gowin I2C to ELVDS IP enables the background update of the I²C bus protocol from I²C to ELVDS, extends single-ended I²C bus transmission to differential bus transmission, and improves transmission distance and anti-interference.

2.2 Features

Gowin I2C to ELVDS IP includes the following features:

- Supports I²C master and slave modes;
- Supports I²C data transmission speed up to 1Mbps;
- Supports I²C 7-bit and 10-bit address mode;
- Supports I²C data background update;
- Supports 3.3V ELVDS operating level;
- Operating clock frequency: 50MHz;
- Supports all series of Gowin FPGA products.

2.3 Resource Utilization

Taking Gowin GW1N-9 device as an instance, its resource utilization is as shown in Table 2-1.

Table 2-1 Performance Reference

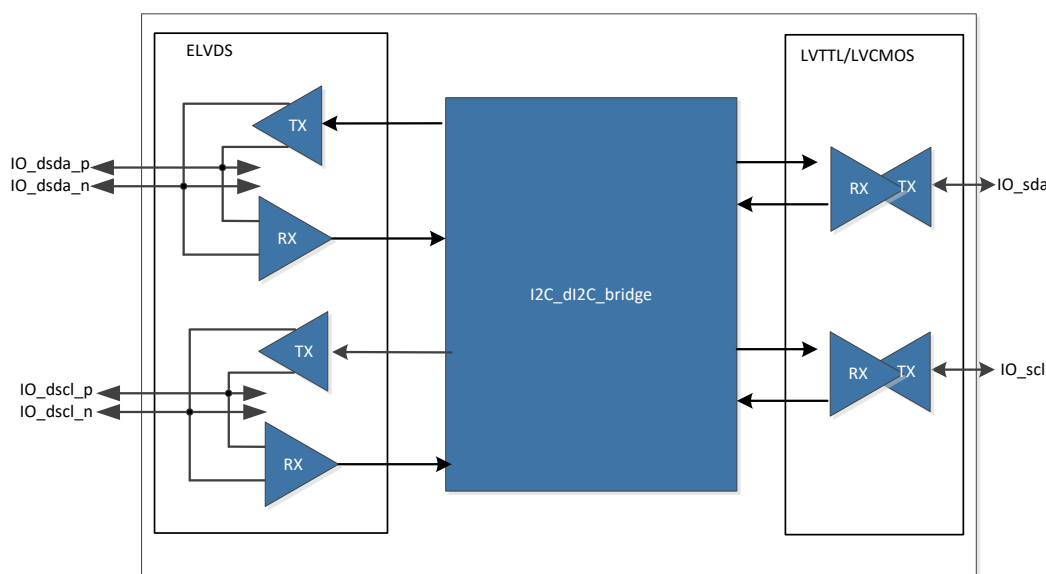
Part Number	Programming Language	LUT4 Resources	REG Resources
GW1N-LV9LQ144C6/I5	Verilog	235	79

3 Functional Description

3.1 I²C to ELVDS Structure Block Diagram

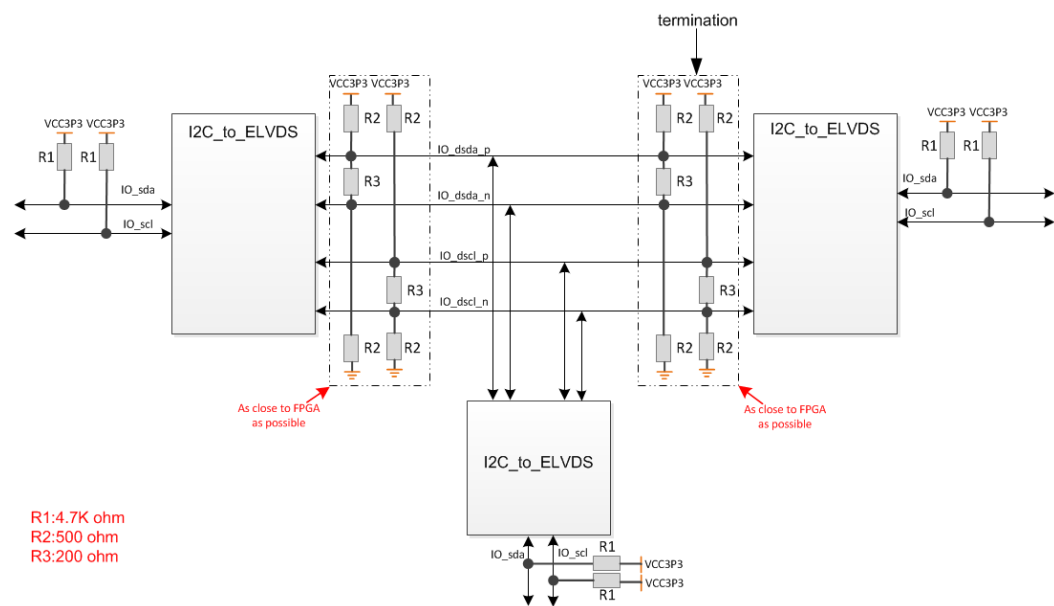
I²C to ELVDS mainly performs the data background upgrade and bridge functions between I²C and differential I²C. The structure block diagram is as follows.

Figure 3-1 Structure Block Diagram



3.2 I²C to ELVDS External Circuit Connection

I²C to ELVDS external circuit connection is as follows.

Figure 3-2 External Resistance Circuit Connection**Note!**

- You can see the followings for the IO port attribute constraints.
 - IO_dsda_p, IO_dsda_n: IO_TYPE=LVDS33E PULL_MODE=NONE DRIVE=8
 - IO_dscl_p, IO_dscl_n: IO_TYPE= LVDS33E PULL_MODE= NONE DRIVE=8
 - IO_i2c_sda: IO_TYPE=LVC MOS33 PULL_MODE= NONE DRIVE=8
 - IO_i2c_scl: IO_TYPE=LVC MOS33 PULL_MODE= NONE DRIVE=8
- The supply voltage of I/O Bank is 3.3V.

4 Signal Definition

4.1 Signal Definition

The signal definition of Gowin I2C to ELVDS IP is as shown in Table 4-1.

Table 4-1 Signal Definition

No.	Signal Name	I/O	Data Width	Description	Note
1	I_clk	I	1	Input clock signal (240MHz)	
2	I_rst_n	I	1	Input reset signal, active-low.	
3	IO_i2c_sda	I/O	1	sda signal on the I ² C	
4	IO_i2c_scl	I/O	1	scl signal on the I ² C	
5	IO_dsda_p	I/O	1	dsda differential signal (+) on the ELVDS	
6	IO_dsda_n	I/O	1	dsda differential signal (-) on the ELVDS	
7	IO_dscl_p	I/O	1	Dscl differential signal (+) on the ELVDS	
8	IO_dscl_n	I/O	1	dscl differential signal (-) on the ELVDS	

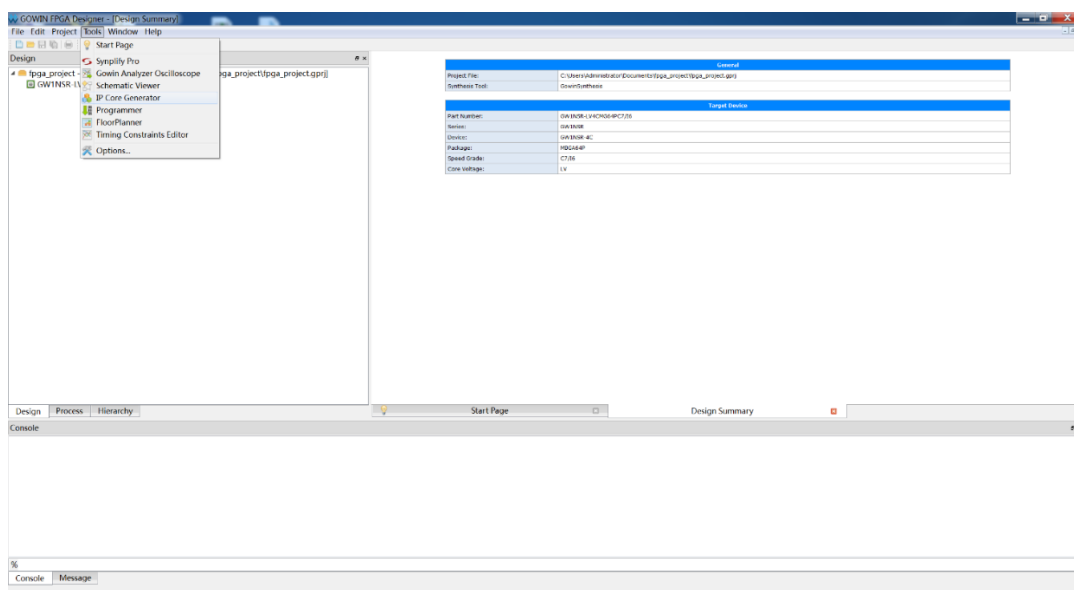
5 Interface Configuration

Click “Tools > IP Core Generator” in the menu bar of Gowin Software interface to call and configure I²C to ELVS.

1. Open IP Core Generator

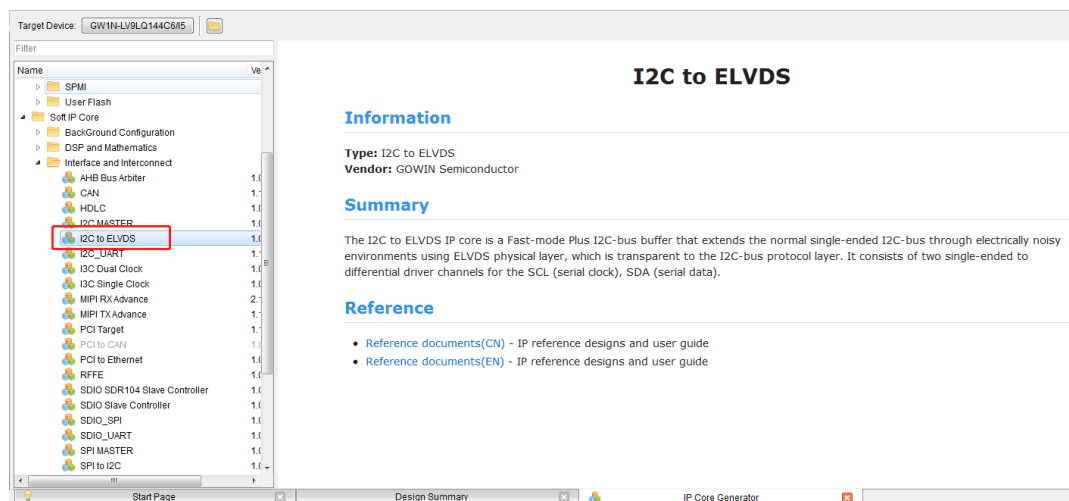
After creating the project, you can click the “Tools” tab in the upper left, then click the “IP Core Generator” via the drop-down list, as shown in Figure 5-1.

Figure 5-1 IP Core Generator



2. Open I2C to ELVDS IP core

Select “Soft IP Core > Interface and Interconnect > I2C_to_ELVDSP”, as shown in Figure 5-2. Double click to open the configuration interface.

Figure 5-2 Open I2C to ELVDS IP Core

3. I2C to ELVDS IP Core Configuration Interface

The configuration interface of I2C to ELVDS IP core is as shown in Figure 5-3. The interface diagram is on the left while the configuration options are on the right.

- You can configure the generated file name in “File Name”.
- You can configure the generated top module name in “Module Name”.

Figure 5-3 I2C to ELVDS IP Configuration Interface