



Gowin SDIO_UART IP User Guide

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1 About This Guide

1.1 Purpose

SDIO-UART user guide mainly includes the features of function, diagram, principle, signal definition, parameter, GUI, and interface timing. It aims to help users quickly understand the features and usage of GowinSDIO-UART to accelerate product development.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com/en.

For the usage of SDIO IP, see [IPUG905](#), *Gowin SDIO Slave Controller User Guide*.

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
SDIO	Secure Digital Input and Output
UART	Universal Asynchronous Receiver/Transmitter

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: <http://www.gowinsemi.com.cn>

E-mail: support@gowinsemi.com

2 Overview

SDIO (Secure Digital Input and Output) defines a peripheral interface on the SD standard.

UART is part of computer hardware that transmits data between serial and parallel communications.

In order to reduce the difficulty of system development and improve the speed of product development SDIO-UART IP is designed to realize the function of interface conversion between SDIO and UART.

After calling the SDIO-UART, it can be applied to GW1N, GW1NR, GW1NS, GW1NZ, GW2A and GW2AR series of FPGA products by using Gowin softwares.

3 Features and Performance

3.1 Features

- Supports data communication of SDIO and UART;
- SDIO interface is slave mode;
- UART supports is 2-wire or 4-wire mode with 1 stop bit, no parity and 8 bit width;
- UART baud rate can be set flexibly by configuring registers;
- Supports up to 4 UART channels;
- Supports interrupt;
- The depth is 64 bytes for UART receiving FIFO;
- The depth is 64 bytes for UART sending FIFO;
- All operations on the user side of SDIO Host can be realized through CMD53 interface, including clearing interrupt registers on the Host side, i.e. reading and writing the Function1 register via CMD53 interface to realize the parameter configuration, state query and data read/write with UART side;
- SDIO CMD53 command OP Code fixed value to 0, select Multi byte R/W to fixed address to complete the data interaction with UART interface;
- Can be synthesized;
- The language is Verilog.

3.2 Performance

The frequency of SDIO-UART depends on the clock frequency provided by the SDIO host and the maximum frequency supported by the IP on the selected chip.

3.3 Resource Utilization

Table 3-1 Performance Reference

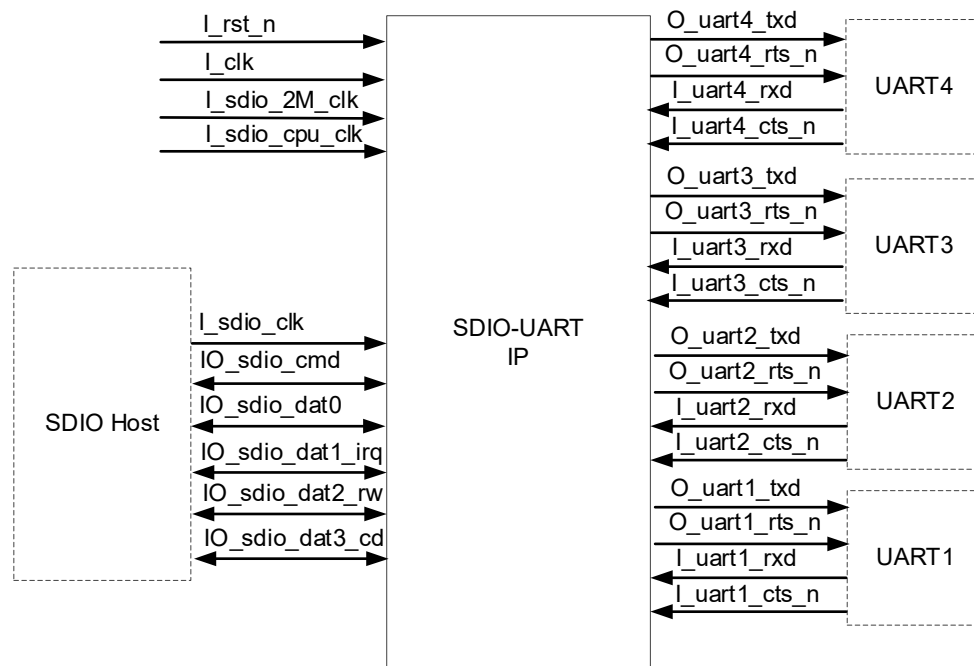
Chip Type	Programming Language	LUT4 Resources	REG Resources
GW2A-LV18PG256C7/I6	Verilog	6313	3289

4 System Block Diagram

4.1 System Block Diagram

SDIO-UART is an interface between SDIO host and UART terminal. It realizes data communication from SDIO UART. SDIO host includes clock, data, command, interrupt SDIO signal. UART signal includes receiving data, transmitting data and flow control signal. SPI_UART includes reset and clock signals.

Figure 4-1 System Block Diagram



Note!

- Normally, the UART interface side triggers the SDIO Host side to operate through interrupts; after the SDIO Host side disables all interrupts in the interrupt register, the SDIO Host can read the status and control the data sending and receiving operations through queries.
- If the interrupt function is enabled, when the UART interface side triggers the interrupt and you receive the interrupt, you should first query the IIR status value

and then execute the corresponding operation according to the instruction of the IIR (it is also OK if you skips the interrupt), and finally you can send a clear interrupt instruction to notify the UART interface side to clear the interrupt.

5 Port List

5.1 System Signal

Table 5-1 System Signal

No.	Signal Name	I/O	Description	Notes
1	I_rst_n	I	Reset	The I/O of all the signals takes IP as reference
2	I_clk	I	System clock for internal logic and UART interface processing	
3	I_sdio_2M_clk	I	SDIO slave required clock	
4	I_sdio_cpu_clk	I	SDIO slave required clock	

5.2 SDIO Signal

Table 5-2 SDIO Side Signal

No.	Signal Name	I/O	Description	Notes
1	I_sdio_clk	I	SDIO clock input	The I/O of all the signals takes IP as reference
2	IO_sdio_cmd	IO	SDIO Command/ Response Signal	
3	IO_sdio_dat0	IO	The SDIO 1bit mode is input of dat signal and the SDIO 4bit mode is input of dat0 signal	
4	IO_sdio_dat1_irq	IO	The SDIO 1bit mode is the input of interrupt signal and the SDIO 4bit mode is the input of dat1 and interrupt multiplexed signal	
5	IO_sdio_dat2_rw	IO	The SDIO 1bit mode is the input of Read Wait signal and the SDIO 4bit mode is the input of dat2 and Read Wait multiplexed signal	
6	IO_sdio_dat3_cd	IO	The SDIO 1bit mode is not defined and the SDIO 4bit mode is the input of dat0	

5.3 UART Signal

Table 5-3 UART4 Signal

No.	Signal Name	I/O	Description	Notes
1	I_uart4_rxd	I	Input serial data	The I/O of all the signals takes IP as reference
2	O_uart4_txd	O	Output serial data	
3	O_uart4_rts_n	O	Allow to transmit signal	
4	I_uart4_cts_n	I	Opposite port ready signal	

Table 5-4 UART3 Signal

No.	Signal Name	I/O	Description	Notes
1	I_uart3_rxd	I	Input serial data	The I/O of all the signals takes IP as reference
2	O_uart3_txd	O	Output serial data	
3	O_uart3_rts_n	O	Allow to transmit signal	
4	I_uart3_cts_n	I	Opposite port ready signal	

Table 5-5 UART2 Signal

No.	Signal Name	I/O	Description	Notes
1	I_uart2_rxd	I	Input serial data	The I/O of all the signals takes IP as reference
2	O_uart2_txd	O	Output serial data	
3	O_uart2_rts_n	O	Allow to transmit signal	
4	I_uart2_cts_n	I	Opposite port ready signal	

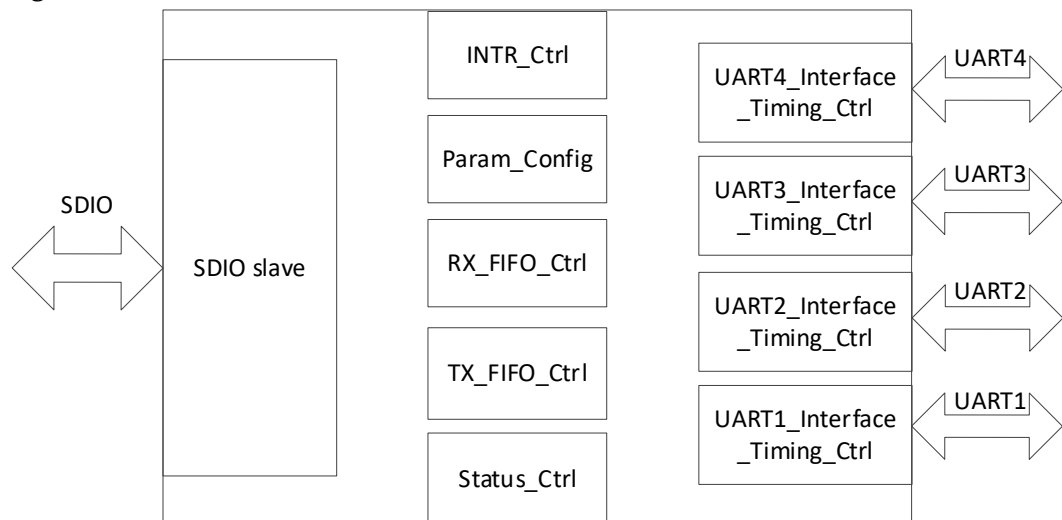
Table 5-6 UART1 Signal

No.	Signal Name	I/O	Description	Notes
1	I_uart1_rxd	I	Input serial data	The I/O of all the signals takes IP as reference
2	O_uart1_txd	O	Output serial data	
3	O_uart1_rts_n	O	Allow to transmit signal	
4	I_uart1_cts_n	I	Opposite port ready signal	

6 Structure and Functional Description

6.1 Architecture

Figure 6-1 Architecture



The IP design includes SDIO_slave, INTR_Ctrl, Param_Config, RX_FIFO_Ctrl, TX_FIFO_Ctrl, Status_Ctrl, UART4_Interface_Timing_Ctrl, UART3_Interface_Timing_Ctrl, UART2_Interface_Timing_Ctrl, UART1_Interface_Timing_Ctrl modules.

- SDIO_slave: Implements data communication with SDIO host and completes SDIO interface timing control and protocol parse;
- INTR_Ctrl: Implement interrupt control function according to IP internal status;
- Param_Config: Receives the configuration parameters from the SDIO host and delivers them to the corresponding module;
- RX_FIFO_Ctrl: Implements data buffer received from UART interface;
- TX_FIFO_Ctrl: Implements data buffer from SDIO host;
- Status_Ctrl: Detects and counts the internal interface status and

working status of IP;

- UART4_Interface_Timing_Ctrl: Realizes data communication with UART4 and completes UART4 interface timing control and protocol parse;
- UART3_Interface_Timing_Ctrl: Realizes data communication with UART3 and completes UART3 interface timing control and protocol parse;
- UART2_Interface_Timing_Ctrl: Realizes data communication with UART2 host and completes UART2 interface timing control and protocol parse;
- UART1_Interface_Timing_Ctrl: Realizes data communication with UART1 and completes UART1 interface timing control and protocol parse.

6.2 Initialization Flow

1. After power on, the SDIO host needs to configure the IP parameters, the recommended sequence is as follows:
 - a) UBDFR4 Register
 - b) UBDFR3 Register
 - c) UBDFR2 Register
 - d) UBDFR1 Register
 - e) MCR Register
 - f) TFCR Register
 - g) RFCR Register
 - h) IITR Register
 - i) IER Register (**Enable register last setting**)
2. Then SDIO host can communicate data with UART according to read/write control operation flow.

6.3 UART Port Write Operation Flow

6.3.1 Disable Interrupt

When the interrupt of sending FIFO register is disabled, the write operation flow from SDIO Host is as follows (Take UART1 for an instance):

1. SDIO Host queries the number of free bytes in the UART1 sending FIFO in the TFLVL register;
2. SDIO Host writes data to the TFR1 register via the CMD53 interface when UART1 sends a FIFO with enough free bytes and the CTS is in a permitted transmit state.
3. The UART1 sending module will then be sent to the link in turn at the set baud rate.

6.3.2 Enable Interrupt

When the interrupt of sending FIFO register is enabled, the write operation flow from UART is as follows (Take UART1 for an instance):

1. The interrupt is triggered when the UART port detects that the number of free bytes in the transmit FIFO is greater than or equal to the Trigger value set by UART1 in the TFCR.
2. After SDIO Host receives an interrupt, it queries the IIR registers through the CMD53 interface.
3. When SDIO Host queries an interrupt of sending FIFO, it will write data to the TFR1 register via the CMD53 interface.
4. After all the data has been written, the SDIO Host side sends a clear interrupt instruction to the UART1 port.
5. Finally, UART1 sending module will be sent to the link sequentially at the set baud rate.

6.4 UART Port Read Operation Flow

6.4.1 Disable Interrupt

When the interrupt of receiving FIFO register is disabled, the read operation flow from SDIO Host is as follows (Take UART1 for an instance):

1. SDIO Host queries the number of received bytes in the UART1 receiving FIFO in the RFLVL register via the CMD53 interface.
2. When there is received data in UART1 receiving FIFO, SDIO Host will read data from RFR1 register through CMD53 interface.

6.4.2 Enable Interrupt

When the interrupt of receiving FIFO register is enabled, the read operation flow from UART1 port is as follows (Take UART1 for an instance):

1. The interrupt is triggered when the UART port detects that the number of bytes received in the receive FIFO is greater than or equal to the Trigger value set by UART1 in the RFCR.
2. After SDIO Host receives an interrupt, it queries the IIR registers through the CMD53 interface.
3. When SDIO Host queries the interrupt of receiving FIFO, it queries the RFLVL register to get the number of received bytes in UART1 receiving FIFO.
4. It then initiates a read data operation from the RFR1 register via the CMD53 interface.
5. After the SDIO Host finishes reading the data, it will send a clear interrupt instruction to UART1 port.

6.5 UART Port Status Query Operation

6.5.1 Disable Interrupt

When the interrupt of Modem status and the interrupt of receiving line status are disabled, SDIO Host initiates the status query operation flow as follows.

When there is received data in the UART receiving FIFO, SDIO Host can query the corresponding receive line and CTS status in the LSR and MSR registers in real time through the CMD53 interface.

6.5.2 Enable Interrupt

When the interrupt of Modem status and the interrupt of receiving line status are enabled, UART initiates the status query operation flow as follows:

1. The UART port triggers an interrupt to notify the SDIO Host when the receiving line status in the LSR and MSR registers of the UART is abnormal or when the CTS changes.
2. After receiving the interrupt, SDIO Host first reads the IIR interrupt register, and then queries the LSR or MSR register through CMD53 interface according to the information, and finally clears the interrupts.

6.6 Register

6.6.1 Register Description

SDIO-UART registers include the following registers:

Table 6-1 Register

No.	Name	Address (17-bit width)	Default (32-bit width)	Type	Description
1	CIR	0x10000	0x00000000	Write	Clearing Interrupt Registers
2	IIR	0x10001	0x00000000	Read/ Write	Interrupt Interval Time Register
3	IER	0x10002	0x00000000	Read/ Write	Interrupt Enable Register
4	UBDFR4	0x10003	0x00000000	Read/ Write	UART4 Baud Rate Frequency Division Register
5	UBDFR3	0x10004	0x00000000	Read/ Write	UART3 Baud Rate Frequency Division Register
6	UBDFR2	0x10005	0x00000000	Read/ Write	UART2 Baud Rate Frequency Division Register
7	UBDFR1	0x10006	0x00000000	Read/ Write	UART1 Baud Rate Frequency Division

No.	Name	Address (17-bit width)	Default (32-bit width)	Type	Description
					Register
8	MCR	0x10007	0x00000000	Read/ Write	Modem Control Register
9	TFCR	0x10008	0x40404040	Read/ Write	Sending FIFO Control Register
10	RFCR	0x10009	0x01010101	Read/ Write	Receiving FIFO Control Register
11	TFR4	0x1000a	--	Write	UART4 Sending FIFO Register
12	TFR3	0x1000b	--	Write	UART3 Sending FIFO Register
13	TFR2	0x1000c	--	Write	UART2 Sending FIFO Register
14	TFR1	0x1000d	--	Write	UART1 Sending FIFO Register
15	IIR	0x00000	0x00000000	Read	Interrupt Identification Register
16	RFR4	0x00001	--	Read	UART4 Receiving FIFO Register
17	RFR3	0x00002	--	Read	UART3 Receiving FIFO Register
18	RFR2	0x00003	--	Read	UART2 Receiving FIFO Register
19	RFR1	0x00004	--	Read	UART1 Receiving FIFO Register
20	LSR	0x00005	0x00000000	Read	Receiving Line Status Register
21	MSR	0x00006	0x00000000	Read	Modem Status Register
22	TFLVL	0x00007	0x00000000	Read	Sending FIFO Indicator Register
23	RFLVL	0x00008	0x00000000	Read	Receiving FIFO Indicator Register

6.6.2 Register Description

Table 6-2 CIR

Address	Bit(s)	Default	Type	Description
0x10000	Bit [31:1]	-	-	Reserved
	Bit [0]	0	Write	Bit0: 1 Clear interrupts; When Host's query to clear the interrupt register is received and bit0 sent is 1, SDIO slave pulls down the fun1_interrupt pin to clear the interrupts.

Table 6-3 IITR

Address	Bit(s)	Default	Type	Description
0x10001	Bit [31:16]	-	-	Reserved
	Bit [15:0]	0x0000	Read/ Write	Interrupt trigger interval: Range from 1 to 65535

Table 6-4 IER

Address	bit	Default	Type	Description
0x10002	Bit [31:24]	0x00	Read/ Write	Bit [31:28]: Reserved Bit 27: Receiving line status interrupts, 0: Turn off; 1: Enable Bit 26: Receiving FIFO register interrupts, 0: Turn off; 1: Enable Bit 25: Sending FIFO register interrupts, 0: Turn off; 1: Enable Bit 24: Modem status interrupts, 0: Turn off; 1: Enable
	Bit [23:16]	0x00	Read/ Write	Bit [23:20]: Reserved Bit 19: Receiving line status interrupts, 0: Turn off; 1: Enable Bit 18: Receiving FIFO register interrupts, 0: Turn off; 1: Enable Bit 17: Sending FIFO register interrupts, 0: Turn off; 1: Enable Bit 16: Modem status interrupts, 0: Turn off; 1: Enable
	Bit [15:8]	0x00	Read/ Write	Bit [15:12]: Reserved Bit 11: Receiving line status interrupts, 0: Turn off; 1: Enable Bit 10: Receiving FIFO register interrupts, 0: Turn off; 1: Enable Bit9: Sending FIFO register interrupts, 0: Turn off; 1: Enable Bit8: Modem status interrupts, 0: Turn off; 1: Enable
	Bit [7:0]	0x00	Read/ Write	Bit [7:4]: Reserved Bit 3: Receiving line status interrupts, 0: Turn off; 1: Enable

Address	bit	Default	Type	Description
				Bit 2: Receiving FIFO register interrupts, 0: Turn off; 1: Enable Bit 1: Sending FIFO register interrupts, 0: Turn off; 1: Enable Bit 0: Modem status interrupts, 0: Turn off; 1: Enable

Table 6-5 UBDFR4

Address	bit	Default	Type	Description
0x10003	Bit [31:16]	-	-	Reserved
	Bit [15:0]	0x0000	Read/ Write	UART4 Baud Rate: Range from 0 to 65525; UART4 Baud Rate Frequency = Input Clock Frequency/ (Frequency Division Register +10)

Table 6-6 UBDFR3

Address	bit	Default	Type	Description
0x10004	Bit [31:16]	-	-	Reserved
	Bit [15:0]	0x0000	Read/ Write	UART4 baud rate: Range from 0 to 65525; UART4 Baud Rate Frequency = Input Clock Frequency/ (Frequency Division Register +10)

Table 6-7 UBDFR2

Address	bit	Default	Type	Description
0x10005	Bit [31:16]	-	-	Reserved
	Bit [15:0]	0x0000	Read/ Write	UART2 Baud Rate: Range from 0 to 65525; UART4 Baud Rate Frequency = Input Clock Frequency/ (Frequency Division Register +10)

Table 6-8 UBDFR1

Address	bit	Default	Type	Description
0x10006	Bit [31:16]	-	-	Reserved
	Bit [15:0]	0x0000	Read/ Write	UART1 Baud Rate: Range from 0 to 65525; UART4 Baud Rate Frequency = Input Clock Frequency/ (Frequency Division Register +10)

Table 6-9 MCR

Address	bit	Default	Type	Description
0x10007	Bit [31:24]	0x00	Read/ Write	Bit [31:26]: Reserved Bit 25: UART4 Transceiver Loopback 0: Normal data communication; 1: Loopback on Bit 24: RTS4 Control 0: Drive RTS to high; 1: Drive RTS to low
	Bit [23:16]	0x00	Read/ Write	Bit [23:18]: Reserved Bit 17: UART3 Transceiver Loopback 0: Normal data communication; 1: Loopback on Bit 16: RTS3 Control 0: Drive RTS to high; 1: Drive RTS to low
	Bit [15:8]	0x00	Read/ Write	Bit [15:10]: Reserved Bit 9: UART2 Transceiver Loopback 0: Normal data communication; 1: Loopback on Bit8: RTS2 Control 0: Drive RTS to high; 1: Drive RTS to low
	Bit [7:0]	0x00	Read/ Write	Bit [7:2]: Reserved Bit 1: UART1 Transceiver Loopback 0: Normal data communication; 1: Loopback on Bit 0: RTS1 Control 0: Drive RTS to high; 1: Drive RTS to low Note! A low RST indicates reception is ready.

Table 6-10 TFCR

Address	bit	Default	Type	Description
0x10008	Bit [31:24]	0x40	Read/ Write	The value of the remaining space Triger for UART4 sending FIFO ranges from 1 to 64 (byte).
	Bit [23:16]	0x40	Read/ Write	The value of the remaining space Triger for UART3 sending FIFO ranges from 1 to 64 (byte).
	Bit [15:8]	0x40	Read/ Write	The value of the remaining space Triger for UART2 sending FIFO ranges from 1 to 64 (byte).
	Bit [7:0]	0x40	Read/ Write	The value of the remaining space Triger for UART1 sending FIFO ranges from 1 to 64 (byte).

Table 6-11 RFCR

Address	bit	Default	Type	Description
0x10009	Bit [31:24]	0x01	Read/ Write	The value of the remaining space Triger for UART4 receiving FIFO ranges from 1 to 64 (byte).
	Bit [23:16]	0x01	Read/ Write	The value of the remaining space Triger for UART3 receiving FIFO ranges from 1 to 64 (byte).
	Bit [15:8]	0x01	Read/ Write	The value of the remaining space Triger for UART2 receiving FIFO ranges from 1 to 64 (byte).
	Bit [7:0]	0x01	Read/ Write	The value of the remaining space Triger for UART1 receiving FIFO ranges from 1 to 64 (byte).

Table 6-12 TFR4

Address	bit	Default	Type	Description
0x1000a	Bit [7:0]	-	Read/ Write	The maximum depth of UART4 sending FIFO is 64 bytes.

Table 6-13 TFR3

Address	bit	Default	Type	Description
0x1000b	Bit [7:0]	-	Read/ Write	The maximum depth of UART3 sending FIFO is 64 bytes.

Table 6-14 TFR2

Address	bit	Default	Type	Description
0x1000c	Bit [7:0]	-	Read/ Write	The maximum depth of UART2 sending FIFO is 64 bytes.

Table 6-15 TFR1

Address	bit	Default	Type	Description
0x1000d	Bit [7:0]	-	Read/ Write	The maximum depth of UART1 sending FIFO is 64 bytes.

Table 6-16 IIR

Address	bit	Default	Type	Description
0x00000	Bit [31:6]	-	-	Reserved
	Bit [5:4]	00		Bit [5:4]: 11: Receiving line status Interrupt (Highest priority) 10: Receiving FIFO status interrupt (Second priority) 01: Sending FIFO status interrupt (Third priority) 00: Modem status interrupt (lowest priority)
	Bit [3:0]	0000	Read-only	Bit [3:0]: 1000: UART4 interrupt is waiting 0100: UART3 interrupt is waiting 0010: UART2 interrupt is waiting 0001: UART1 interrupt is waiting 0000: no interrupt Others: reserved

Table 6-17 RFR4

Address	bit	Default	Type	Description
0x00001	Bit [7:0]	-	Read-only	The maximum depth of UART4 receiving FIFO is 64 bytes.

Table 6-18 RFR3

Address	bit	Default	Type	Description
0x00002	Bit [7:0]	-	Read-only	The maximum depth of UART3 receiving FIFO is 64 bytes.

Table 6-19 RFR2

Address	bit	Default	Type	Description
0x00003	Bit [7:0]	-	Read-only	The maximum depth of UART2 receiving FIFO is 64 bytes.

Table 6-20 RFR1

Address	bit	Default	Type	Description
0x00004	Bit [7:0]	-	Read-only	The maximum depth of UART1 receiving FIFO is 64 bytes.

Table 6-21 LSR

Address	bit	Default	Type	Description
0x00005	Bit [31:24]	0x00	Read-only	Bit [31:27]: Reserved Bit 26: 0: No communication interrupt 1: Communication interrupt detected. Clear after read Bit 25: 0: No frame errors, 1: Frame errors detected. Clear after read Bit 24: 0: Receiving FIFO without overflow, 1: Receiving FIFO detected overflow; Clear after read
	Bit [23:16]	0x00	Read-only	Bit [23:19]: Reserved Bit 18: 0: No communication interrupt, 1: Communication interrupt detected; Clear after read Bit 17: 0: No frame errors, 1: Frame errors detected. Clear after read Bit 16: 0: Receiving FIFO without overflow, 1: Receiving FIFO detected overflow; Clear after read
	Bit [15:8]	0x00	Read-only	Bit [15:11]: Reserved Bit 10: 0: No communication interrupt, 1: Communication interrupt detected; Clear after read Bit 9: 0: No frame error, 1: Frame errors detected; Clear after read Bit 8: 0: Receiving FIFO without overflow, 1: Receiving FIFO detected overflow; Clear after read
	Bit [7:0]	0x00	Read-only	Bit [7:3]: Reserved Bit 2: 0: No communication interrupt, 1: Communication interrupt detected; Clear after read Bit 1: 0: No frame errors, 1: Frame errors detected; Clear after read Bit 0: 0: Receiving FIFO without overflow, 1: Receiving FIFO detected overflow; Clear after read

Table 6-22 MSR

Address	bit	Default	Type	Description
0x00006	Bit [31:24]	0x00	Read-only	Bit [31:26]: Reserved Bit 25: CTS4 signal status (Active-high, indicating that the opposite end is ready to receive). Bit 24: CTS4 signal state change indication (Active-high), clear after read
	Bit [23:16]	0x00	Read-only	Bit [23:18]: Reserved Bit 17: CTS3 signal status (Active-high, indicating that the opposite end is ready to receive). Bit 16: CTS3 signal state change indication (Active-high), clear after read
	Bit [15:8]	0x00	Read-only	Bit [3:10 PM]: Reserved Bit 9: CTS2 signal status (Active-high, indicating that the opposite end is ready to receive). Bit 8: CTS2 signal state change indication (Active-high), clear after read
	Bit [7:0]	0x00	Read-only	Bit [7:2]: Reserved Bit 1: CTS1 signal status (Active-high, indicating that the opposite end is ready to receive). Bit 0: CTS1 signal state change indication (Active-high), clear after read

Table 6-23 TFLVL

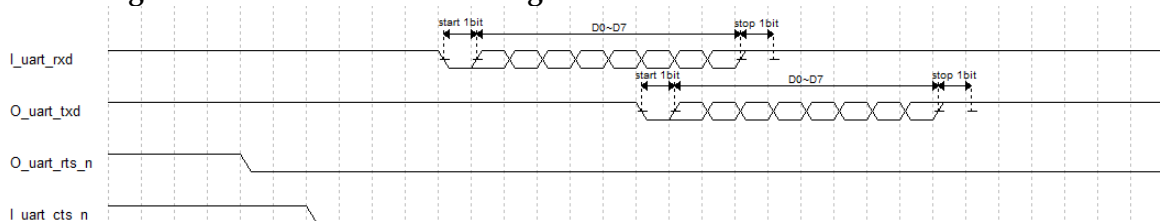
Address	bit	Default	Type	Description
0x00007	Bit [31:24]	0x00	Read-only	The value of the number of valid data in UART4 sending FIFO ranges from 0 to 64 (byte)
	Bit [23:16]	0x00	Read-only	The value of the number of valid data in UART3 sending FIFO ranges from 0 to 64 (byte)
	Bit [15:8]	0x00	Read-only	The value of the number of valid data in UART2 sending FIFO ranges from 0 to 64 (byte)
	Bit [7:0]	0x00	Read-only	The value of the number of valid data in UART1 sending FIFO ranges from 0 to 64 (byte)

Table 6-24 RFLVL

Address	bit	Default	Type	Description
0x00008	Bit [31:24]	0x00	Read-only	The value of the number of valid data in UART4 receiving FIFO ranges from 0 to 64 (byte)
	Bit [23:16]	0x00	Read-only	The value of the number of valid data in UART4 receiving FIFO ranges from 0 to 64 (byte)
	Bit [15:8]	0x00	Read-only	The value of the number of valid data in UART4 receiving FIFO ranges from 0 to 64 (byte)
	Bit [7:0]	0x00	Read-only	The value of the number of valid data in UART4 receiving FIFO ranges from 0 to 64 (byte)

6.7 Interface Timing

6.7.1 UART Interface Timing (4 Mode)

Figure 6-2 UART Interface Timing

6.7.2 SDIO Bus Interface

It is compliant with standard SDIO bus protocol and timing.

7 Parameters Configuration

7.1 Overview

GUI parameter definition for SDIO-UART.

7.2 Parameter

Uart4 channel	Uart4 channel select : Yes or No Default: No
Uart4 4wire mode	Uart4 4wire mode select: Yes or No Default: No
Uart3 channel	Uart3 channel select : Yes or No Default: No
Uart3 4wire mode	Uart3 4wire mode select: Yes or No Default: No
Uart2 channel	Uart2 channel select : Yes or No Default: No
Uart2 4wire mode	Uart2 4wire mode select: Yes or No Default: No
Uart1 channel	Uart1 channel select : Yes or No Default: No
Uart1 4wire mode	Uart1 4wire mode select: Yes or No Default: No

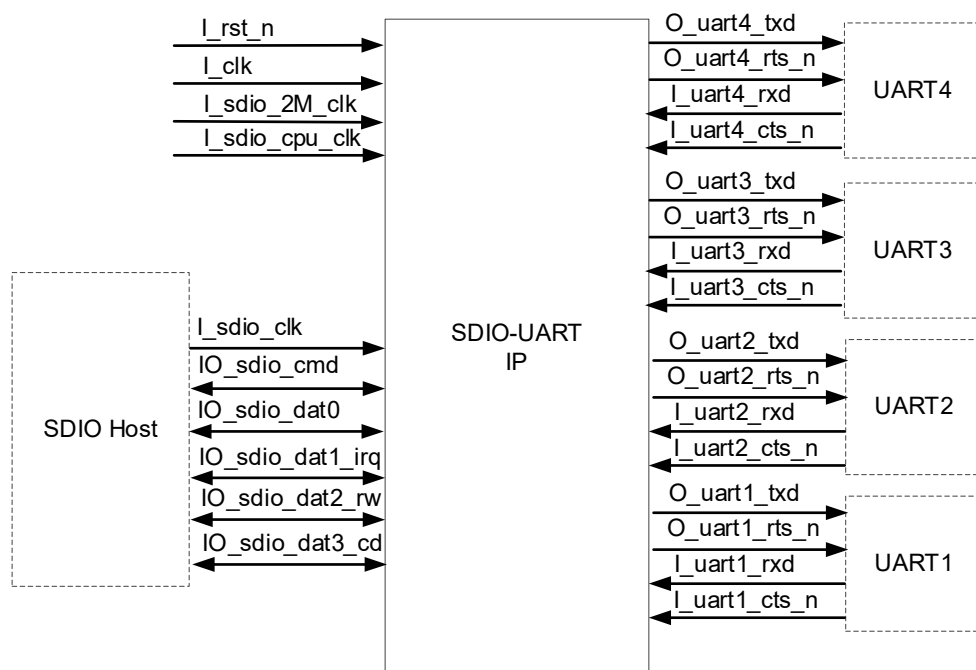
8 Interface Configuration

8.1 Overview

It mainly introduces how to set parameters and generate usable SDIO-UART Module through GUI interface.

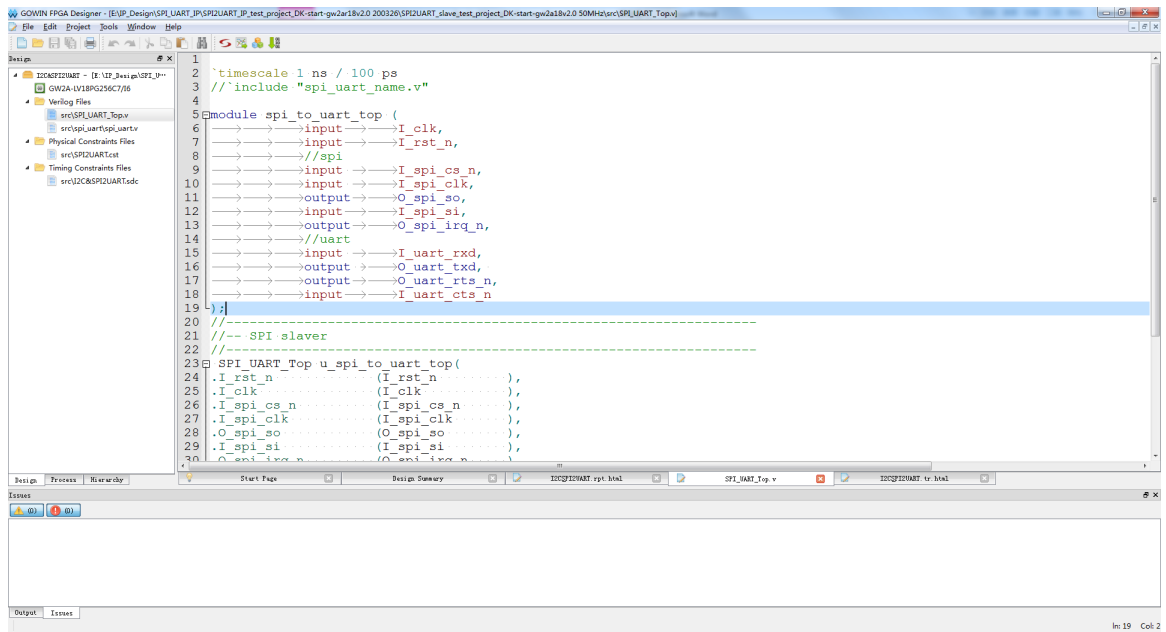
8.2 Application Diagram

Figure 8-1 Application Diagram

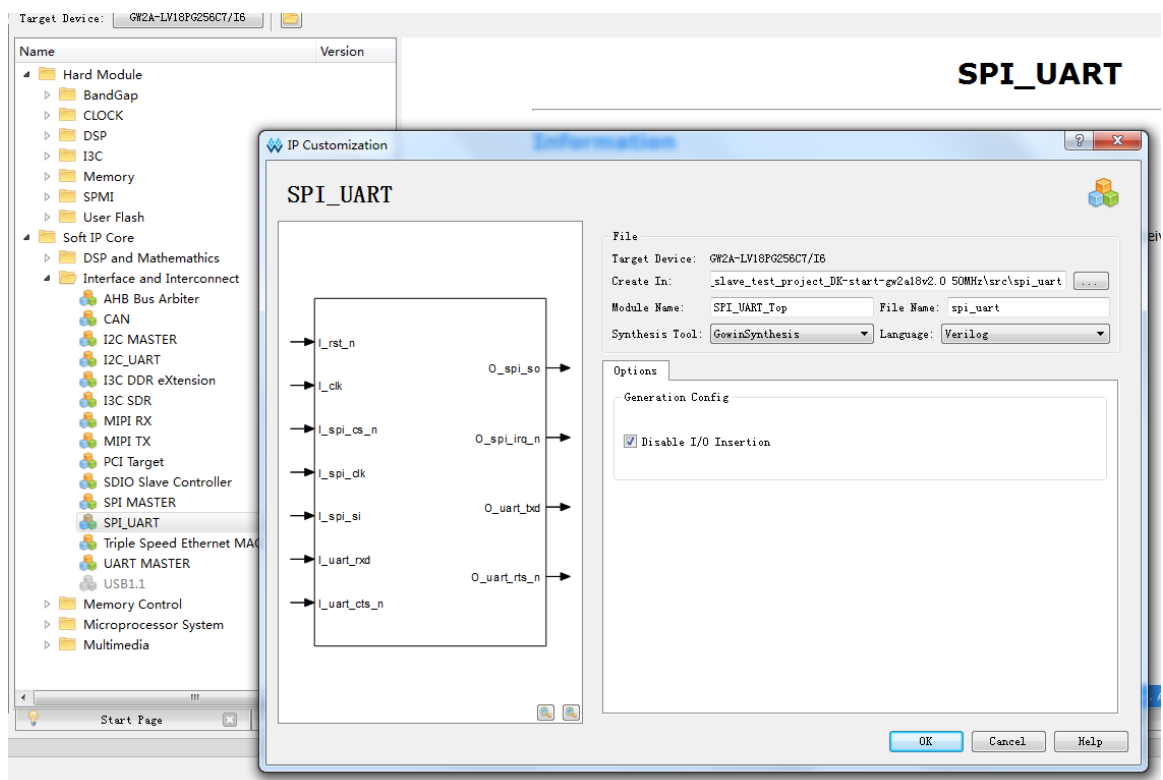


8.3 GUI Call

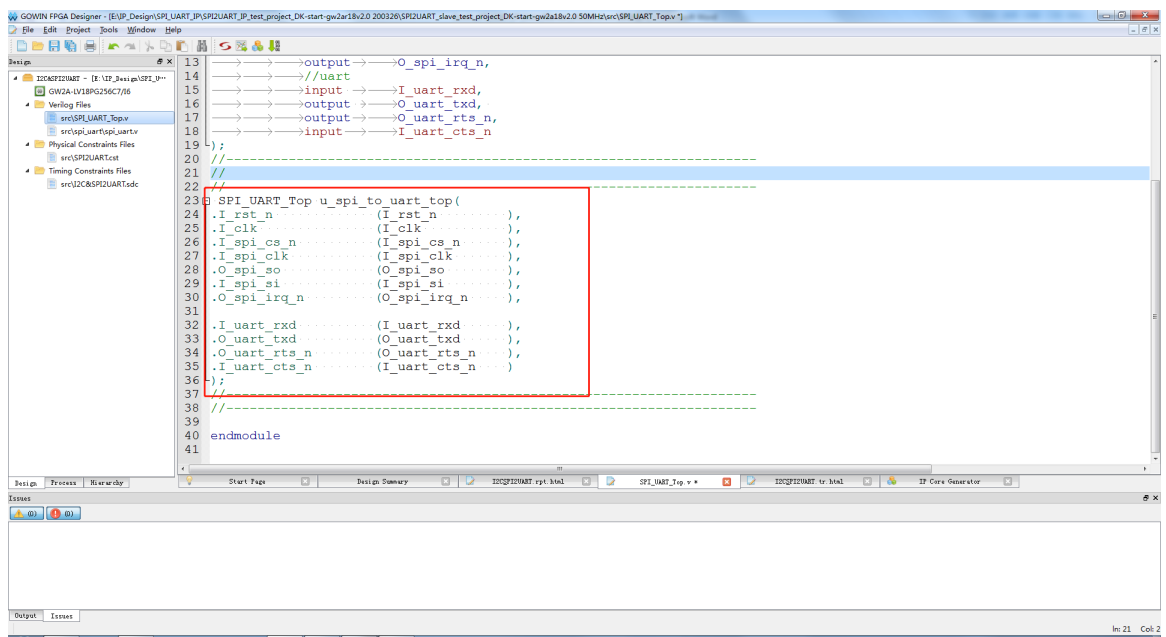
1. Start the Gowin Software and open an project, as shown below:



2. Click "IP Core Generator" from the Tools menu, as shown below: Click the "OK" to generate the SDIO_UART Module.



3. Instantiate SDIO_UART in the user application, as shown below .



Synthesize, P&R, download bitstream file to FPGA chip to implement SDIO- UART function.

