



Gowin FOC Current Loop Control IP

Release Note

RN942-1.0E, 07/02/2020

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Revision History

Date	Version	Description
07/02/2020	1.0E	Initial version published.

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About This Guide

This release includes Gowin FOC Current Loop Control IP user guide.

Gowin FOC Current Loop Control IP user guide and reference design are available at Gowin Website. Take specific parameters as an example for the reference design, which can be used for simulation and download test after synthesis, placement and routing.

Overview

Gowin FOC Current Loop Control IP can realize FOC current loop design to control the motor. IP has four kinds of mode to meet different design demands.

Table 1 Gowin FOC Current Loop Control IP Overview

Gowin FOC Current Loop Control IP	
Supported Devices	GW1N series of FPGA products: GW1N-4, GW1N-4B, GW1N-9, GW1N-9C; GW1NR series of FPGA products: GW1NR-4, GW1NR-4B, GW1NR-9, GW1NR-9C; GW2A series of FPGA products; GW2AR series of FPGA products.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	Gowin Software

Documents

This software release includes Gowin FOC Current Loop Control IP documents, which are listed below:

Table 2 Documents List

Documents	Usage
IPUG942, Gowin FOC Current Loop Control User Guide.pdf	PDF
RN942, Gowin FOC Current Loop Control Release Note.pdf	PDF

IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and users can determine the location and timing constraints on their own.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com

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