



Gowin FOC Current Loop Control

User Guide

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Revision History

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Contents

Contents	i
List of Figures	iii
List of Tables	iv
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Overview	3
2.1 Introduction to FOC Current Loop Control IP	3
2.2 Features and Performance	3
2.2.1 Features	3
2.2.2 Max. Frequency	4
2.2.3 Latency	4
2.2.4 Resource Utilization	4
3 Functional Description	5
3.1 Introduction to FOC Current Loop Control Algorithm	5
3.1.1 Principle of Motor	5
3.1.2 Principle of FOC and Current Loop	6
3.1.3 Principle of Clarke Transform	8
3.1.4 Principle of Park Transform	8
3.1.5 Principle of Inverse Park Transform	9
3.1.6 Principle of PI Control	9
3.1.7 Principle of SVPWM	10
3.2 Structure and Function	12

3.3 Port Description	14
3.4 Timing Description	16
3.4.1 Basic Transform Mode Timing	16
3.4.2 Basic Transform + SVPWM Mode Timing	17
3.4.3 Basic Transform + PI Control Mode Timing	18
3.4.4 Basic Transform + PI + SVPWM Mode Timing	18
4 GUI.....	20
5 Reference Design.....	23

List of Figures

Figure 3-1 Motor Schematic.....	5
Figure 3-2 Schematic of Three-phase Bridge Driven by Motor	6
Figure 3-3 FOC Schematic	7
Figure 3-4 FOC Current Loop Schematic	7
Figure 3-5 Clarke Transform Schematic	8
Figure 3-6 Clarke Transform Schematic	8
Figure 3-7 Inverse Park Transform Schematic	9
Figure 3-8 PI Control Schematic.....	9
Figure 3-9 Anti-Windup PI Schematic	10
Figure 3-10 SVPWM Sectors.....	10
Figure 3-11 Schematic of Three-phase Bridge Driven by Motor.....	10
Figure 3-12 Sectors	11
Figure 3-13 Synthesized Vector of First Sector	11
Figure 3-14 PWM Output of First Sector	12
Figure 3-15 Implementation Block Diagram of FOC Current Loop Control	13
Figure 3-16 Four Modes	14
Figure 3-17 I/O Ports Diagram of FOC Current Loop Control IP	15
Figure 3-18 Basic Transform Mode Timing	17
Figure 3-19 Basic Transform + SVPWM Mode Timing	17
Figure 3-20 Basic Transform + PI Control Mode Timing.....	18
Figure 3-21 Basic Transform + PI + SVPWM ModeTiming	19
Figure 4-1 IP Core Generator GUI.....	20
Figure 4-2 FOC Current Loop Control GUI	21
Figure 4-3 Help	22
Figure 5-1 Block Diagram of Reference Design	23

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 2-1 Gowin FOC Current Loop Control IP	3
Table 2-2 Resource Utilization	4
Table 3-1 Switch Order of Sectors	12
Table3-2 I/O List of FOC Current Loop Control	15

1 About This Guide

1.1 Purpose

The purpose of Gowin FOC Current Loop Control IP User Guide is to help users learn the features and usage of Gowin FOC Current Loop Control IP by providing the description of the product overview, functional description, GUI and reference design.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. [DS100](#), GW1N series of FPGA Products Data Sheet
2. [DS117](#), GW1NR series of FPGA Products Data Sheet
3. [DS102](#), GW2A series of FPGA Products Data Sheet
4. [DS226](#), GW2AR series of FPGA Products Data Sheet
5. [SUG100](#), Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
DSP	Digital Signal Processing
IP	Intellectual Property
RAM	Random Access Memory
LUT	Look-up Table
FOC	Field Oriented Control
SVPWM	Space Vector Pulse Width Modulation

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to FOC Current Loop Control IP

Gowin FOC Current Loop Control IP can realize FOC current loop design to control the motor. IP has four kinds of mode to meet different design demands.

Table 2-1 Gowin FOC Current Loop Control IP

Gowin FOC Current Loop Control IP	
Supported Devices	GW1N series of FPGA products: GW1N-4, GW1N-4B, GW1N-9 and GW1N-9C; GW1NR series of FPGA products: GW1NR-4, GW1NR-4B, GW1NR-9 and GW1NR-9C; GW2A series of FPGA products; GW2AR series of FPGA products.
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify Pro
Application Software	Gowin Software

2.2 Features and Performance

2.2.1 Features

- Four modes to select;
- PI control module and SVPWM module to select;
- Data width: 16, 18, 24, 32;
- Low delay.

2.2.2 Max. Frequency

The maximum frequency of Gowin FOC Current Loop Control IP is mainly determined by the speed grade of the devices, and it can reach up to 85M.

2.2.3 Latency

The latency of FOC Current Loop Control IP is determined by the configuration parameters.

2.2.4 Resource Utilization

FOC Current Loop Control is implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, grade or the different modes of IP configuration.

Take the GW2A-18 series of FPGA as an example. See Table 2-2 for the resource utilization. For the applications on the other GOWINSEMI devices, see the later release.

Table 2-2 Resource Utilization

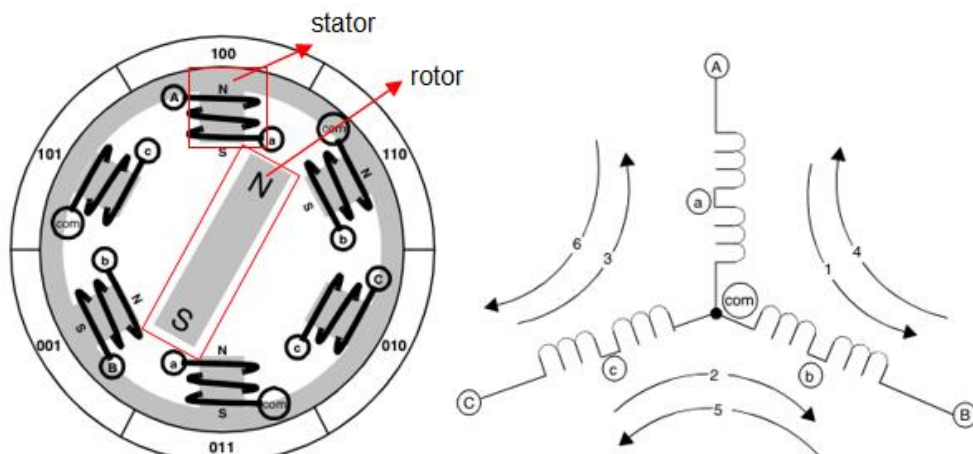
Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW2A18	-7	LUT	1692	● Basic+PIControl+SVPWM Mode; ● Data width is 18 bits, and fraction width is 17 bits.
		ALU	1055	
		REG	886	
		BSRAM	0	
		DSP	10	

3 Functional Description

3.1 Introduction to FOC Current Loop Control Algorithm

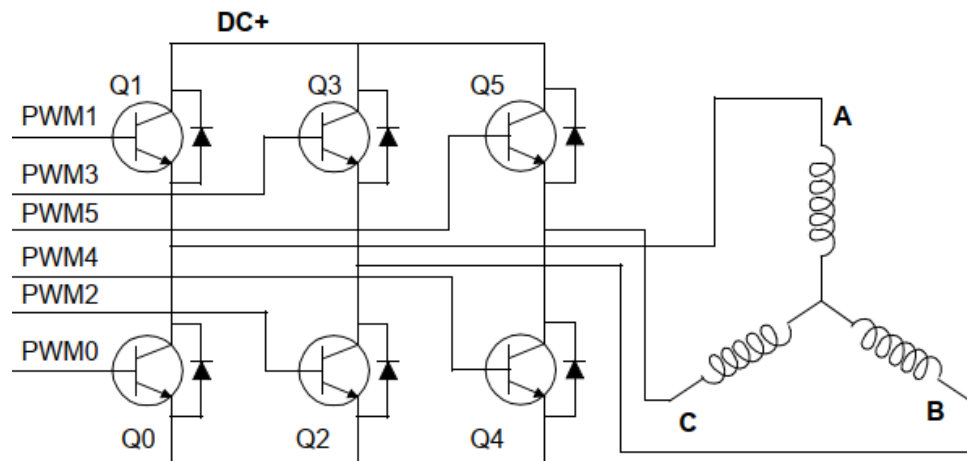
3.1.1 Principle of Motor

Figure 3-1 Motor Schematic



A motor is an electromagnetic device that converts or transfers electric energy according to the law of electromagnetic induction. It can produce drive torque as a power source for electrical appliances or machines.

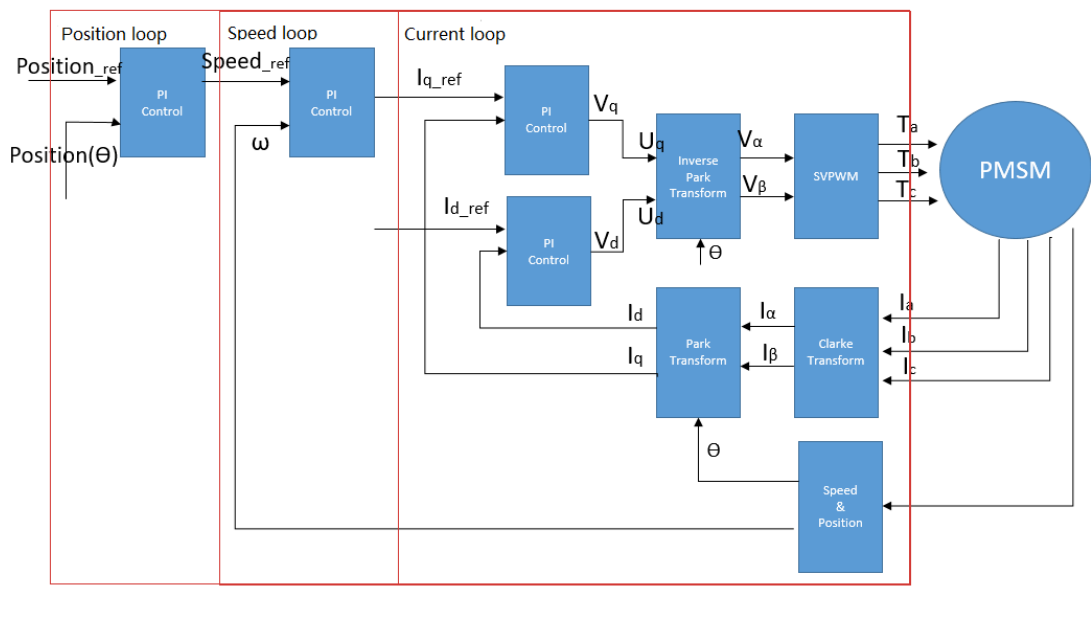
The motor consists of stator and rotor. The motor consists of two parts: stator and rotor. The rotation of the motor causes the current flowing through the winding stator to produce a magnetic field. The three-phase bridge flows through the periodic current, allowing the rotor to rotate for one cycle.

Figure 3-2 Schematic of Three-phase Bridge Driven by Motor

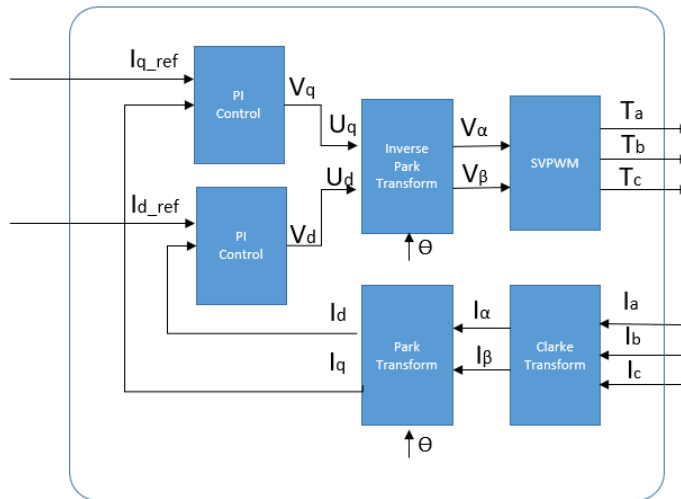
The three-phase bridge driven by motor-driven is shown in Figure 3-2. By turning on/off the switches, the magnetic field is produced by energizing the A, B and C to make the rotor rotate. For example, if Q1 and Q4 on and others off, the positive current flows from Q1 to the A-phase winding stator, then the C-phase winding stator and flows back from Q4 to the negative pole. The current flows through the A and C stator winding will produce a magnetic field. According to electromagnetic induction and right hand law, it can be seen that the direction is parallel to B. Therefore, the rotor turns to the parallel position of B. To make the motor rotate continuously in a specified direction, the stator must be energized in a certain order.

3.1.2 Principle of FOC and Current Loop

FOC, also called vector control, controls the excitation current and torque current of the motor by measuring and controlling the stator current vector.

Figure 3-3 FOC Schematic

FOC control is as shown in Figure 3-3. FOC control includes inner loop control (current loop) and outer loop control (position loop and speed loop). The outer loop control obtains the speed and position by the Hall sensor of the motor to control the speed and position of motor. FOC inner loop control is the core of FOC.

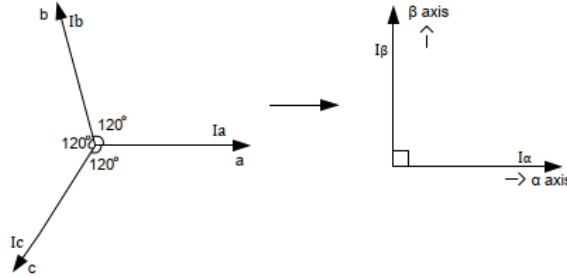
Figure 3-4 FOC Current Loop Schematic

The inner loop control is the core of FOC. FOC current loop control is a process of converting three-phase current to mutually quadrature current, as shown in Figure 3-4. The three-phase current of the motor is input through ADC sampling. The three-phase stationary coordinate system is converted to two-phase rotating coordinate system by Clarke transform and Park transform. The speed is adjusted by PI control; the coordinate

system is restored by inverse Park transform; The voltage is controlled to output to PWM and three-phase bridge by SVPWM for motor drive control.

3.1.3 Principle of Clarke Transform

Figure 3-5 Clarke Transform Schematic



Clarke transform is a process of transforming a three-axis two-dimensional coordinate system to a two-axis two-dimensional coordinate system, as shown in Figure 3-5.

$$I_{\alpha} = \frac{2}{3}I_a - \frac{1}{3}I_b - \frac{1}{3}I_c$$

$$I_{\beta} = \frac{1}{\sqrt{3}}(I_b - I_c)$$

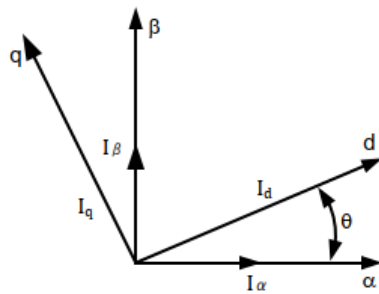
If $I_a + I_b + I_c = 0$, then

$$I_{\alpha} = I_a$$

$$I_{\beta} = \frac{1}{\sqrt{3}}(I_b + 2I_c)$$

3.1.4 Principle of Park Transform

Figure 3-6 Clarke Transform Schematic



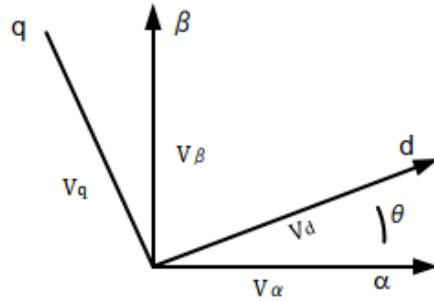
Park transform is to convert the stationary coordinate system to a rotating coordinate system, as shown in Figure 3-6.

$$I_d = I_{\alpha} \cos(\theta) + I_{\beta} \sin(\theta)$$

$$I_q = I_\beta \cos(\theta) - I_\alpha \sin(\theta)$$

3.1.5 Principle of Inverse Park Transform

Figure 3-7 Inverse Park Transform Schematic



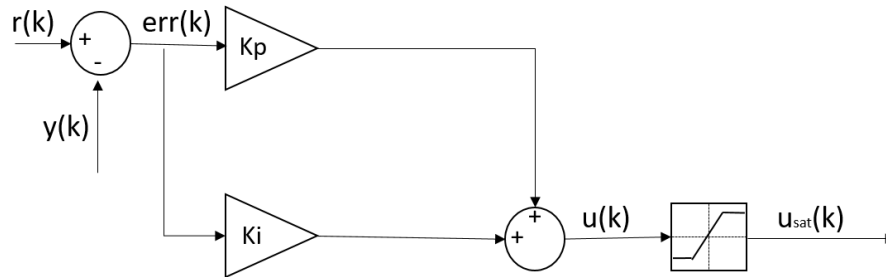
Inverse Park transform is to convert the rotational coordinate system to a stationary coordinate system, as shown in Figure 3-7.

$$V_\alpha = V_d \cos(\theta) - V_q \sin(\theta)$$

$$V_\beta = V_q \cos(\theta) + V_d \sin(\theta)$$

3.1.6 Principle of PI Control

Figure 3-8 PI Control Schematic

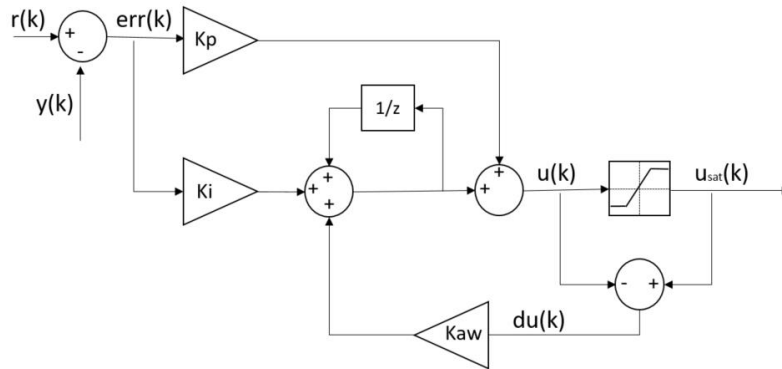


$$u(k) = Kp * err(k) + Ki * err(k)$$

PI control controls the error by proportional factor Kp and integral factor Ki , as shown in Figure 3-8. The actual value $r(k)$ and the reference value $y(k)$ generate $err(k)$.

PI control is usually designed in a linear region, which does not take into account the input limit of the control object, resulting in error output, and the closed-loop system will produce the corresponding instability, which is called the Wind-up. In order to solve this problem, the PI controller of Anti-Windup is designed as shown in Figure 3-9.

Figure 3-9 Anti-Windup PI Schematic



$$u(k) = Kp * err(k) + \left(Ki + Kaw * du(k) \frac{z}{z-1} \right) err(k)$$

The PI control of Anti-Windup reduces the influence of integrator by feeding back the error of input and output to integrator to suppress wind-up phenomenon.

3.1.7 Principle of SVPWM

SVPWM space vector pulse width modulation is a reference coordinate system with the stator of the three-phase motor as the ideal magnetic chain. By controlling the three-phase bridge tube, thus producing the PWM waveform approximating the ideal magnetic chain.

Figure 3-10 SVPWM Sectors

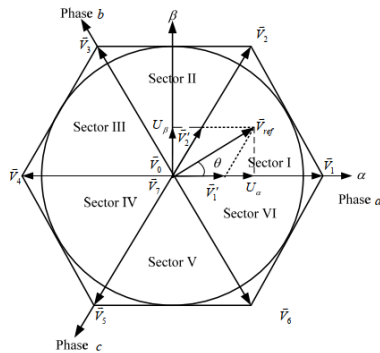
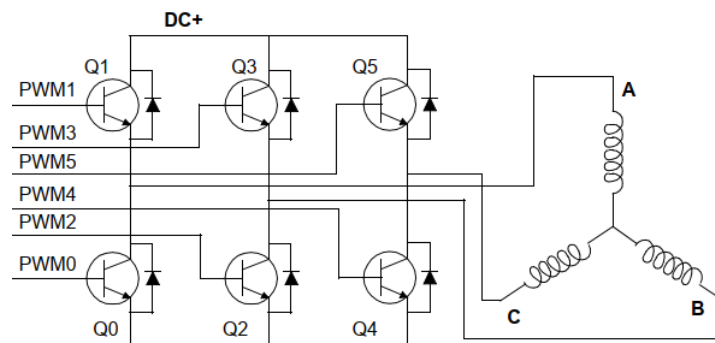


Figure 3-11 Schematic of Three-phase Bridge Driven by Motor



SVPWM divides the space into six sectors, and each sector corresponds to the three-phase bridge switching tube by encoding (A, B, C). 0 indicates that the upper tube is closed and the lower tube is open, and 1 indicates that the upper tube is open and the lower tube is closed. For example, sector (1, 0, 0) indicates that Q1, Q2, Q4 are open and other are closed. The rotor is rotated to the desired angular position of the sector 1 by controlling the switching current.

Figure 3-12 Sectors

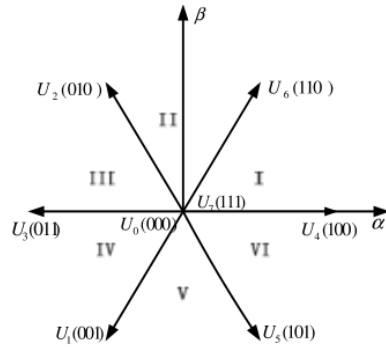
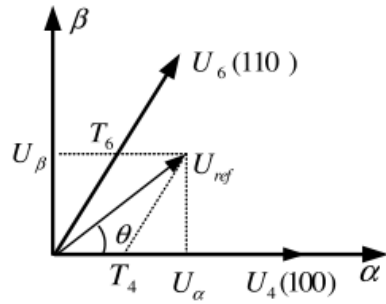


Figure 3-13 Synthesized Vector of First Sector



The expected output voltage of U_{ref} is obtained by vector synthesis of U_1T_1 and U_3T_3 .

$$\int_0^T U_{ref} = \int_0^{T_4} U_4 + \int_{T_4}^{T_4+T_6} U_6 + \int_{T_4+T_6}^T U_0$$

$$U_{out} T = U_4 T_4 + U_6 T_6 + U_0 T_{T-T_4-T_6} = U_x T_x + U_y T_y + U_0 T_0$$

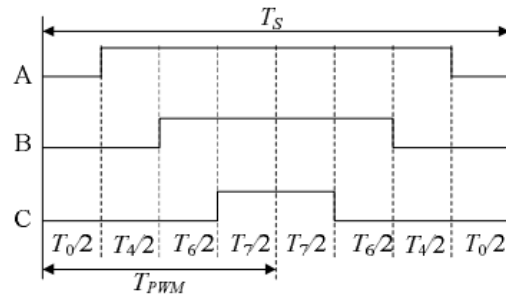
Where U_{ref} is the expected output voltage, T is the cycle. T_x , T_y , T_0 is the time of corresponding coordinate system and zero vector U_0 in one cycle.

The actual pulse width modulation waveform is obtained by calculating the vector switch time. Zero vector selection is more flexible, and the appropriate choice can reduce the number of switching. Avoiding the switching at the time of high load current can minimize the switch loss.

Therefore, with the goal of reducing the number of switching, the allocation of the basic vector is as follows: In every switching, only the switching of one phase is changed, and the zero vector is equally distributed in time so that the generated PWM is symmetrical and the harmonic component of PWM is effectively reduced.

Taking the first sector as an example, the voltage vector is U_0 , U_4 , U_6 , U_7 , U_7 , U_6 , U_4 , U_0 , and PWM output is as below.

Figure 3-14 PWM Output of First Sector



The switch order of other sectors is as shown below.

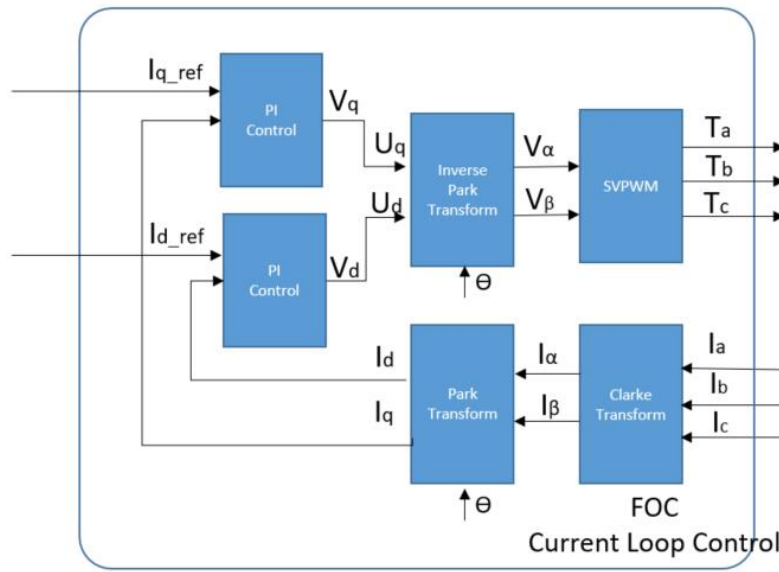
Table 3-1 Switch Order of Sectors

Sector	U_{ref} Position	Order
I	$0 \leq \theta \leq 60$	...0-4-6-7-7-6-4-0...
II	$60 \leq \theta \leq 120$	...0-2-6-7-7-6-2-0...
III	$120 \leq \theta \leq 180$	...0-2-3-7-7-3-2-0...
IV	$180 \leq \theta \leq 240$	...0-1-3-7-7-3-1-0...
V	$240 \leq \theta \leq 300$	...0-1-5-7-7-5-1-0...
vi	$300 \leq \theta \leq 360$	...0-4-5-7-7-5-4-0...

3.2 Structure and Function

Gowin FOC Current Loop Control implementation block diagram is shown in Figure 3-15.

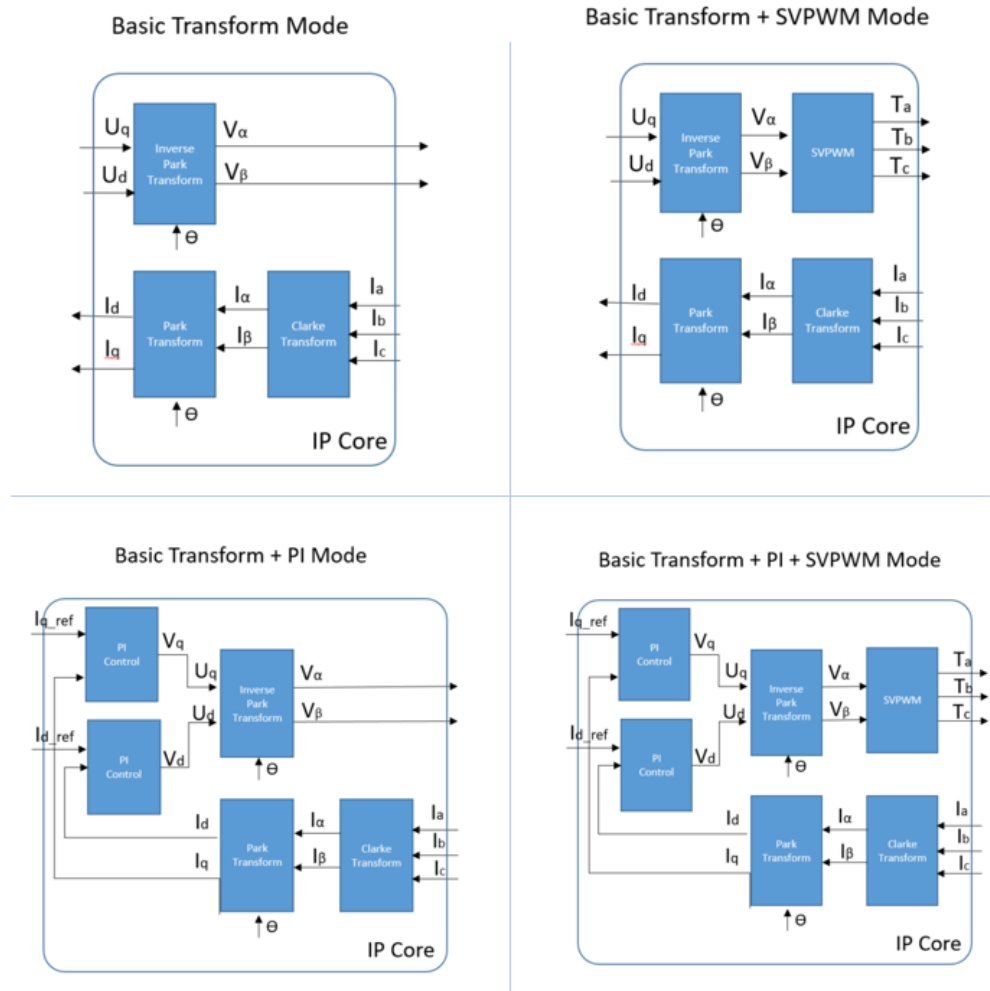
Figure 3-15 Implementation Block Diagram of FOC Current Loop Control



It consists of the following modules.

1. Clarke Transform: The phase current I_a I_b I_c sampled by ADC is converted from three-axis to two-axis coordinate system, and it outputs I_α and I_β .
2. Park Transform: Converts the static coordinates of I_α and I_β to the rotational coordinate system, and it outputs I_d and I_q .
3. PI Control: Controls the proportion and integral of error generated by I_q , I_d , I_{q_ref} and I_{d_ref} , and it outputs U_q and U_d .
4. Inverse Park Transform: Converts the rotational coordinates of the U_q and U_d to a stationary coordinate system, and it outputs U_α and U_β .
5. SVPWM: Performs SVPWM algorithm according to U_α and U_β , and it outputs phase vector time T_a , T_b and T_c .

Figure 3-16 Four Modes



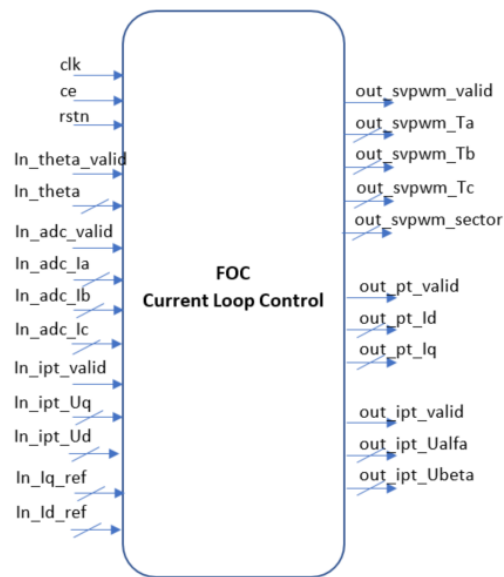
As shown in Figure 3-16, FOC current loop control includes four modes:

- Basic Transform
- Basic Transform + SVPWM
- Basic Transform + PI
- Basic Transform + PI + SVPWM

3.3 Port Description

The I/O ports diagram of the Gowin FOC Current Loop Control IP is shown in Figure 3-17.

Figure 3-17 I/O Ports Diagram of FOC Current Loop Control IP



The I/O details are shown in Table3-2.

Table3-2 I/O List of FOC Current Loop Control

Signal	I/O	Data Width	Description
clk	Input	1	Clock signal
ce	Input	1	Enable Signal
rstn	Input	1	Reset signal, active - low
In_theta_valid	Input	1	Angle signal input valid
In_theta	Input	18	Angle data is expressed as 0-65536 ° to indicate 0-360°.
In_adc_valid	Input	1	ADC current input valid
In_adc_la	Input	16/18/24/32	ADC Ia
In_adc_lb	Input	16/18/24/32	ADC Ib
In_adc_lc	Input	16/18/24/32	ADC Ic (When Clarke Transform with three inputs, this signal exists)
In_ipt_valid	Input	1	Inverse Park Transform input valid (When there is no PI Control, this signal exists)
In_ipt_Uq	Input	16/18/24/32	Inverse Park Transform inputs Uq (When there is no PI Control, this signal exists)
In_ipt_Ud	Input	16/18/24/32	Inverse Park Transform inputs Ud (When there is no PI Control, this signal exists)
In_lq_ref	Input	16/18/24/32	PI Control inputs Iq (When there is PI Control, this signal exists)
In_ld_ref	1	16/18/24/32	PI Control inputs Id (When there is PI Control, this signal exists)

Signal	I/O	Data Width	Description
Out_svpwm_valid	O	1	SVPWM output valid (When there is SVPWM, this signal exists)
Out_svpwm_Ta	O	16/18/24/32	SVPWM outputs Ta (When there is SVPWM, this signal exists)
Out_svpwm_Tb	O	16/18/24/32	SVPWM outputs Tb (When there is SVPWM, this signal exists)
Out_svpwm_Tc	O	16/18/24/32	SVPWM outputs Tc (When there is SVPWM, this signal exists)
Out_svpwm_sector	O	3	SVPWM sectors (When there is SVPWM, this signal exists)
Out_pt_valid	O	1	Park Transform output valid (When there is no PI Control, this signal exists)
Out_pt_Id	O	16/18/24/32	Park Transform outputs Id (When there is no PI Control, this signal exists)
Out_pt_Iq	O	16/18/24/32	Park Transform outputs Iq (When there is no PI Control, this signal exists)
Out_ipt_valid	O	1	Inverse Park Transform output valid (When there is no SVPWM, this signal exists)
Out_ipt_Ualfa	O	16/18/24/32	Inverse Park Transform outputs Ualfa (When there is no SVPWM, this signal exists)
Out_ipt_Ubeta	O	16/18/24/32	Inverse Park Transform outputs Ubeta (When there is no SVPWM, this signal exists)

Note!

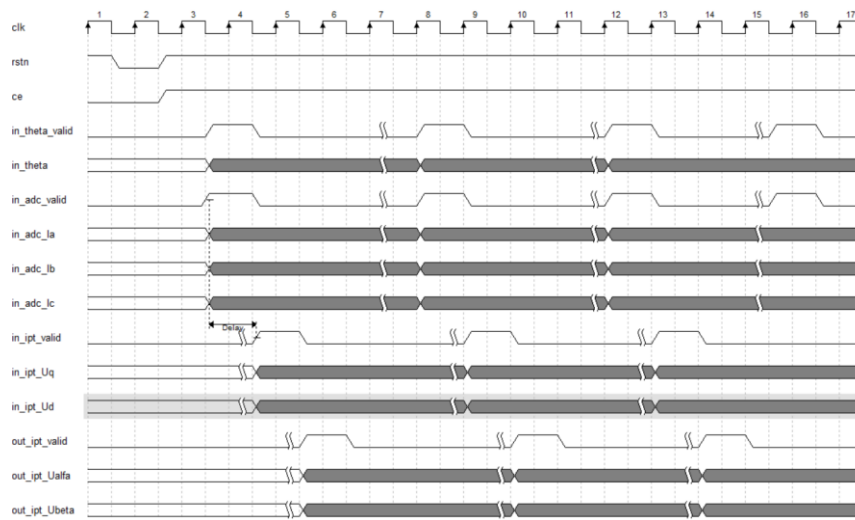
- PI Control module mode refers to Basic Transform + PI Mode and Basic Transform + PI + SVPWM.
- SVPWM module mode refers to Basic Transform + SVPWM and Basic Transform + PI + SVPWM.

3.4 Timing Description

This chapter describes the timing of Gowin FOC Current Loop Control IP.

3.4.1 Basic Transform Mode Timing

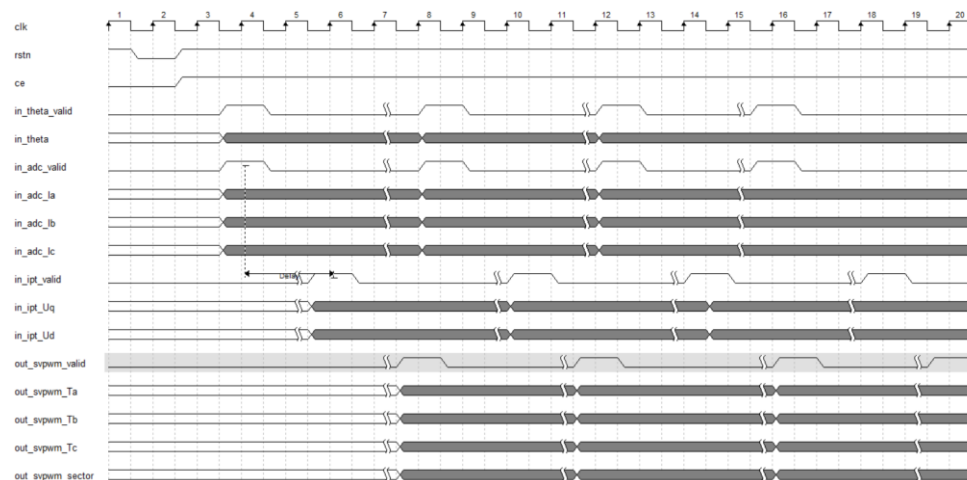
The Basic Transform Mode timing diagram is as shown in Figure 3-18.

Figure 3-18 Basic Transform Mode Timing

1. Angle signal (in_theta) is input at valid pulse signal (in_theta_valid at high level).
2. The three-phase sampling current (in_adc_la, in_adc_lb, in_adc_lc) is input at valid signal (in_adc_valid at high level).
3. After a delay, the inverse Park transform module inputs data (in_ipt_Uq, in_ipt_Ud) at valid pulse signal (in_ipt_valid at high level).
4. After calculation, it outputs data (out_ipt_Ualfa, out_ipt_Ubeta) and valid pulse signal (out_ipt_valid at high level).

3.4.2 Basic Transform + SVPWM Mode Timing

The Basic Transform + SVPWM Mode timing diagram is as shown in Figure 3-19.

Figure 3-19 Basic Transform + SVPWM Mode Timing

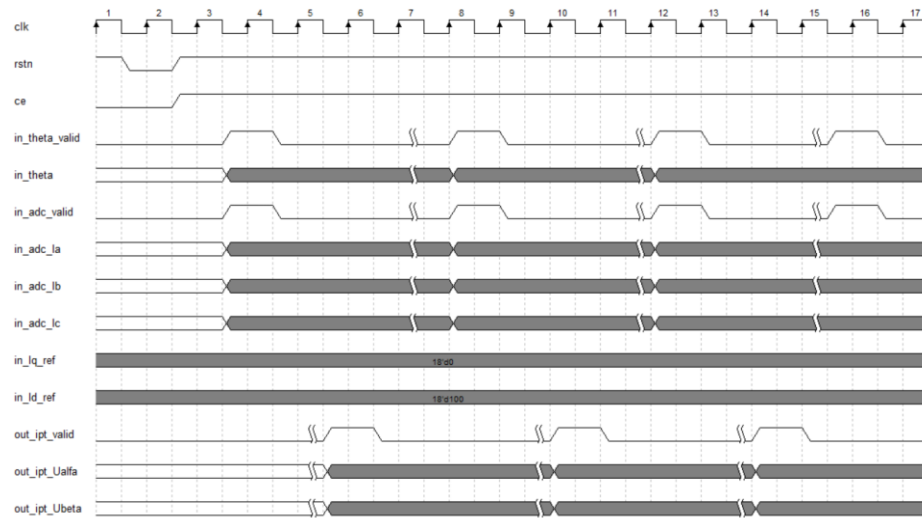
1. Angle signal (in_theta) is input at valid pulse signal (in_theta_valid at high level).

2. The three-phase sampling current (in_adc_la, in_adc_lb, in_adc_lc) is input at valid pulse signal (in_adc_valid at high level).
3. After a delay, the inverse Park transform module inputs data (in_ipt_Uq, in_ipt_Ud) at valid pulse signal (in_ipt_valid at high level).
4. After calculation, it outputs data (out_svpwm_Ta, out_svpwm_Tb, out_svpwm_Tc out_svpwm_sector) and valid signal (out_ipt_valid at high level).

3.4.3 Basic Transform + PI Control Mode Timing

The Basic Transform + PI Control Mode timing diagram is as shown in Figure 3-20.

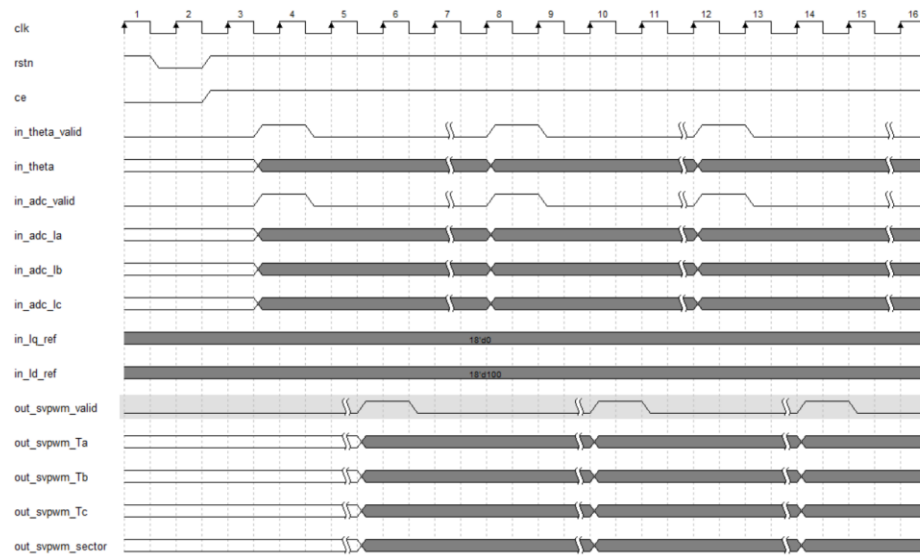
Figure 3-20 Basic Transform + PI Control Mode Timing



1. Angle signal (in_theta) is input at valid pulse signal (in_theta_valid at high level).
2. The three-phase sampling current (in_adc_la, in_adc_lb, in_adc_lc) is input at valid pulse signal (in_adc_valid at high level).
3. Input Iq reference voltage (in_lq_ref) and Id reference voltage (in_ld_ref).
4. After calculation, it outputs data (out_ipt_Ualfa, out_ipt_Ubeta) and valid pulse signal (out_ipt_valid at high level).

3.4.4 Basic Transform + PI + SVPWM Mode Timing

The Basic Transform + PI + SVPWM Mode timing diagram is as shown in Figure 3-21.

Figure 3-21 Basic Transform + PI + SVPWM ModeTiming

1. Angle signal (in_theta) is input at valid pulse signal (in_theta_valid at high level).
2. The three-phase sampling current (in_adc_la, in_adc_lb, in_adc_lc) is input at valid pulse signal (in_adc_valid at high level).
3. Input Iq reference voltage (in_lq_ref) and Id reference voltage (in_ld_ref).
4. After calculation, it outputs data (out_svpwm_Ta, out_svpwm_Tb, out_svpwm_Tc out_svpwm_sector) and valid pulse signal (out_ipt_valid at high level).

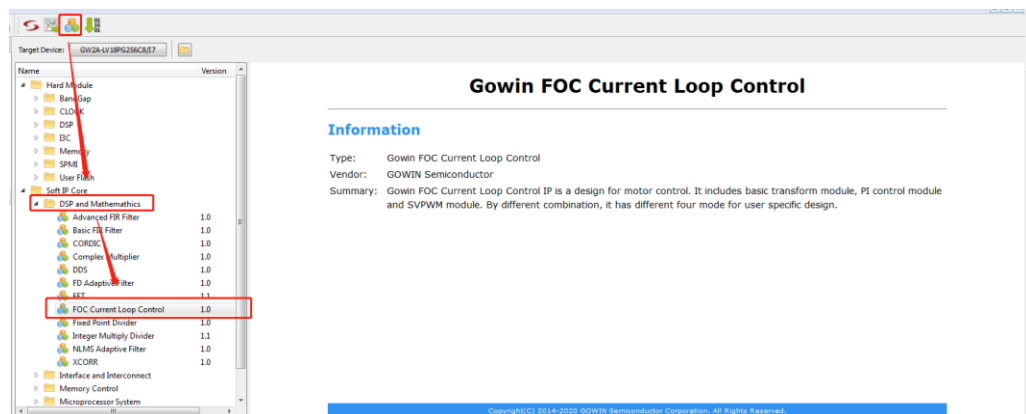
4 GUI

Select Tools in the Gowin software GUI, and it can start the IP Core Generator to invoke and configure FOC Current Loop Control.

1. Open IP Core Generator

After creating a new project, it can click "IP Core Generator" to open the IP Core Generator, as shown in Figure 4-1.

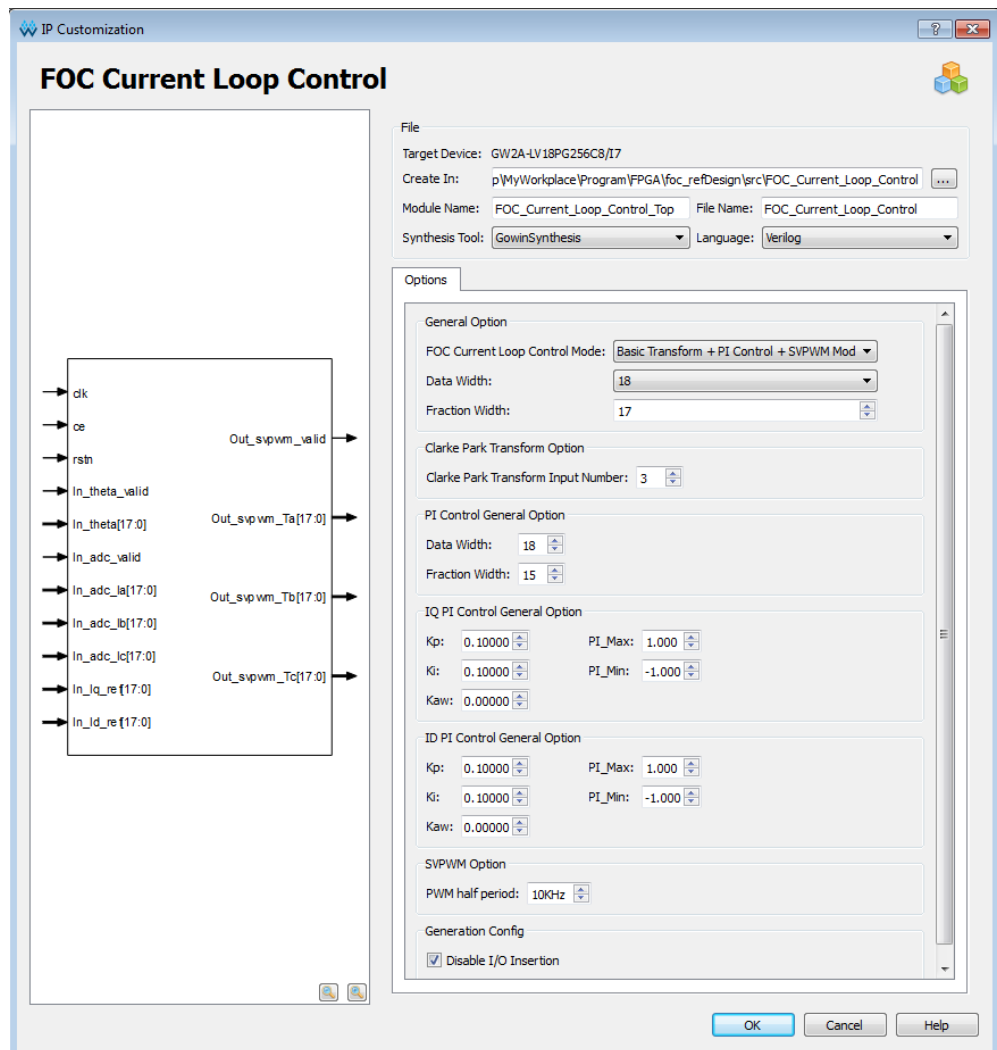
Figure 4-1 IP Core Generator GUI



2. Open FOC Current Loop Control

Click "DSP and Mathematics", then double-click "FOC Current Loop Control" to open GUI, as shown in Figure 4-2.

Figure 4-2 FOC Current Loop Control GUI



3. Configure FOC Current Loop Control

The Options includes General Option, Clarke Transform Option, PI Control Option and SVPWM Option.

- General Option includes IP mode, data width and fraction width.
- Clarke Park Transform Option includes Clarke Park Transform input number (including 2 and 3 inputs)
- PI Control Option includes data width, fraction width, the Kp, KI, Kaw parameters of the IQ PI Control and ID PI Control modules, and the maximum and minimum values.
- SVPWM Option includes the SVPWM half period.

4. Open Help

Click "Help" button in the right lower corner of Figure 4-2 to learn the simple English introduction to options in GUI, so as to help users quickly complete the configuration of IP core. The order of options in Help is the

same as the one in the interface, as shown in Figure 4-3.

Figure 4-3 Help

Gowin FOC Current Loop Control	
Information	
Type:	Gowin FOC Current Loop Control
Vendor:	GOWIN Semiconductor
Summary:	Gowin FOC Current Loop Control IP is a design for motor control. It includes basic transform module, PI control module and SVPWM module. By different combination, it has different four mode for user specific design.
Options	
Option	Description
General Option	
FOC Current Loop Control Mode	FOC Current Loop Control Mode
Data Width	Data width
Fraction Width	Fraction Width
Clarke Park Transform Option	
Clarke Park Transform Input Number	Clarke Park Transform Input Number
PI Control General Option	
Data Width	Data Width
Fraction Width	Fraction Width
IQ PI Control Option	
Kp	The proportional gain coefficient.
Ki	The integral gain coefficient.
Kaw	The anti-windup gain coefficient.
PI_Max	Pi value upper limit
PI_Min	Pi value lower limit
ID PI Control Option	
Kp	The proportional gain coefficient.
Ki	The integral gain coefficient.
Kaw	The anti-windup gain coefficient.
PI_Max	Pi value upper limit
PI_Min	Pi value lower limit
SVPWM Option	
PWM half period	PWM half period
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5 Reference Design

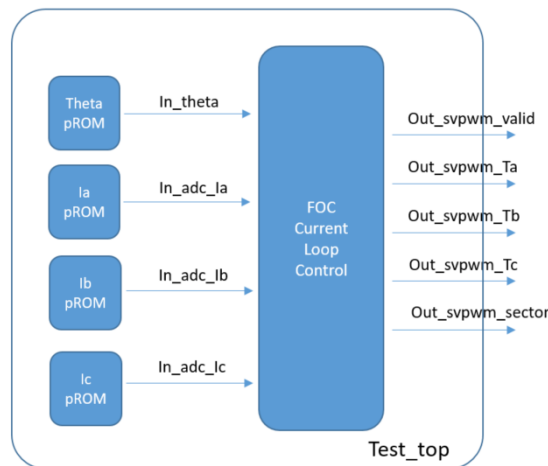
This chapter introduces the usage of FOC Current Loop Control reference design. FOC Current Loop Control design instance has only one module. See the Current Loop Control reference design for details.

Application

The block diagram of reference design is as shown in Figure 5-1. In the design instance, the steps are as follows:

1. The input data (Theta, Ia, Ib, Ic) is stored in pROM, then transmitted to FOC Current Loop Control module.
2. After calculating by FOC Current Loop Control module, the output is obtained.
3. The reference design uses Basic + PI Control + SVPWM Mode.

Figure 5-1 Block Diagram of Reference Design



FOC Current Loop Control functions can be verified using this design. When the reference design is applied to board level test, the users need to provide appropriate incentive to the reference design and use an on-line logic analyzer or oscilloscope to observe the signals.

