



Gowin AEC IP

User Guide

IPUG761-1.2E, 10/17/2025

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Revision History

Date	Version	Description
01/28/2021	1.0E	Initial version published.
12/08/2023	1.0.1E	The range of data width updated.
03/21/2025	1.1E	● Port description updated. ● Resource utilization updated. ● IP features updated. ● NLMS description removed.
05/30/2025	1.1.1E	Figure 4-1 Open the IP Configuration Interface Via Toolbar Icon updated.
10/17/2025	1.2E	● "Threshold" and "Smooth Factor" parameter configuration for "Double Talk Detector" supported. ● Figure 3-1 Gowin AEC IP Structure updated. ● The I/O port diagram updated and the description for the dt_detect port added. ● Descriptions for the configuration options added.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	2
1.4 Support and Feedback	2
2 Overview	3
2.1 Introduction to Gowin AEC IP	3
2.2 Features	3
2.3 Max. Frequency	3
2.4 Latency	4
2.5 Resource Utilization	4
3 Functional Description	5
3.1 Gowin AEC IP Structure	5
3.2 Algorithm Introduction	5
3.3 Port Description	7
3.4 Timing Description	8
4 Interface Configuration	9
5 Reference Design	11
6 File Delivery	12
6.1 Document	12
6.2 Design Source Code (Encryption)	12
6.3 Reference Design	12

List of Figures

Figure 3-1 Gowin AEC IP Structure	5
Figure 3-2 Gowin AEC IP Port Diagram.....	7
Figure 3-3 Gowin AEC IP Mode Timing Diagram	8
Figure 4-1 Open the IP Configuration Interface Via Toolbar Icon	9
Figure 4-2 Gowin AEC IP Configuration Interface	10

List of Tables

Table 1-1 Terminology and Abbreviations	2
Table 2-1 Gowin AEC IP Overview	3
Table 2-2 Gowin AEC IP Resource Utilization	4
Table 3-1 Algorithm Variable List.....	6
Table 3-2 Gowin AEC IP IO Description.....	7
Table 4-1 Configuration Options	10
Table 6-1 Document List	12
Table 6-2 AEC Design Source Code List	12
Table 6-3 Gowin AEC IP RefDesign File List	12

1 About This Guide

1.1 Purpose

The purpose of Gowin AEC IP User Guide is to help you learn the features and usage of Gowin AEC IP by providing the descriptions of the product overview, functional description, GUI and reference design. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.11.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find related documents at www.gowinsemi.com

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AEC	Acoustic Echo Cancellation
BSRAM	Block Static Random Access Memory
DSP	Digital Signal Processing
IP	Intellectual Property
LUT	Look-up Table

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Introduction to Gowin AEC IP

Gowin Acoustic Echo Cancellation (AEC) IP can perform echo cancellation on the input signals. This IP employs an APF (Affine Projection Filter), which adaptively adjusts its coefficients to minimize errors and filter out highly correlated echo components in the captured signal when the Double Talk Detector does not detect double-talk, thereby achieving echo cancellation. The input signal x and the desired signal d must be of the same size. In Gowin AEC IP, the projection order of the APF is fixed at 2, while the filter length and the parameters of the Double-Talk Detector are user-configurable.

Table 2-1 Gowin AEC IP Overview

Gowin AEC IP	
Logic Resource	Please refer to Table 2-2.
Delivered Doc.	
Design Files	Verilog (encrypted)
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.7.01Beta and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.2 Features

- Supports 16-bit fixed-point input
- Supports configurable filter length
- Supports the threshold and smooth factor parameter configuration for Double-talk Detector

2.3 Max. Frequency

The maximum frequency of Gowin AEC IP is primarily determined by the device used and the speed grade of the devices. Taking GW5A-25 series of FPGA for an instance, it can reach up to 90 MHz.

2.4 Latency

The output latency of Gowin AEC IP is primarily determined by the configuration parameters.

2.5 Resource Utilization

Gowin AEC IP performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds or the different modes of IP configuration.

Taking Gowin GW5A-25 series of FPGA for an instance, the resource utilization is shown in Table 2-2. For application verification on other Gowin FPGA, please pay attention to the later release information.

Table 2-2 Gowin AEC IP Resource Utilization

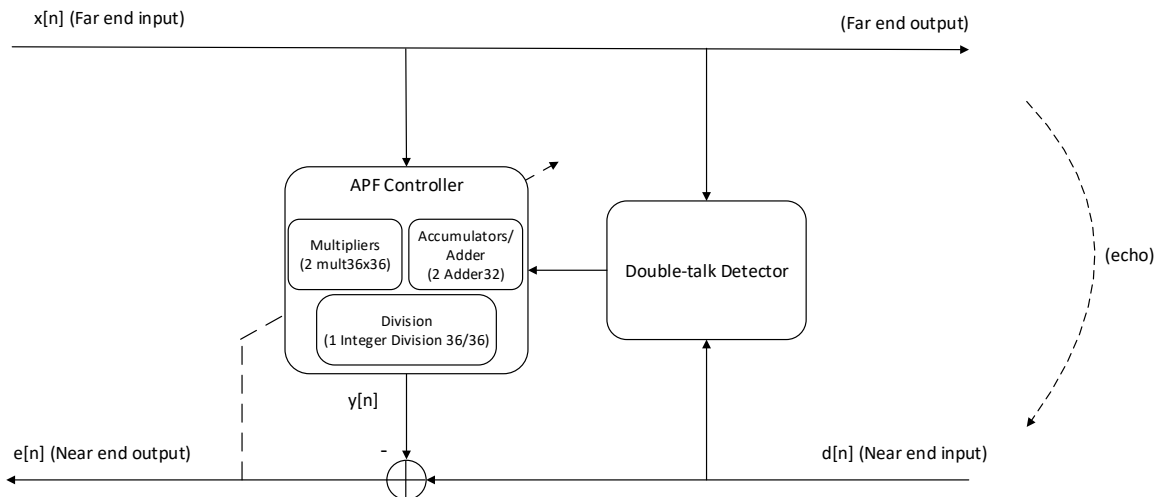
Device Series	Speed Grade	Resource Utilization	
GW5A-25	ES	BSRAM	3
		SSRAM	0
		Registers	1484
		LUTs	1899
		ALUs	326
		MULT27X36	4

3 Functional Description

3.1 Gowin AEC IP Structure

Gowin AEC IP structure diagram is as shown in Figure 3-1.

Figure 3-1 Gowin AEC IP Structure



3.2 Algorithm Introduction

The Affine Projection Filter algorithm reuses past input data, allowing faster convergence when the input signals are highly correlated. This results in a class of algorithms that balance computational complexity and convergence speed. The formulas of the algorithm are shown below:

$$X_{ap}(n) = \begin{pmatrix} x(n) & x(n-1) \\ \vdots & \vdots \\ x(n-N) & x(n-1-N) \end{pmatrix}$$

$$y_{ap}(n) = X^T(n)w(n)$$

$$d_{ap}(n) = \begin{pmatrix} d(n) \\ d(n-1) \end{pmatrix}$$

$$e_{ap}(n) = d_{ap}(n) - y_{ap}(n)$$

$$w(n) = w(n-1) + \left(X_{ap}(n) \left(X_{ap}^T(n) X_{ap}(n) + \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \right)^{-1} \right) e_{ap}$$

Double talk detector evaluates the short-term power of the near-end and far-end inputs using an exponential moving average, based on the following formula:

$$x_{ma} = \alpha \times x_{ma} + (1 - \alpha) \times |x(n)|$$

$$d_{ma} = \alpha \times d_{ma} + (1 - \alpha) \times |d(n)|$$

When the volume ratio of the far-end input to the near-end input exceeds the configured threshold, double-talk is detected, and the filter coefficient update is suspended.

$$d_{ma} < T \times x_{ma}$$

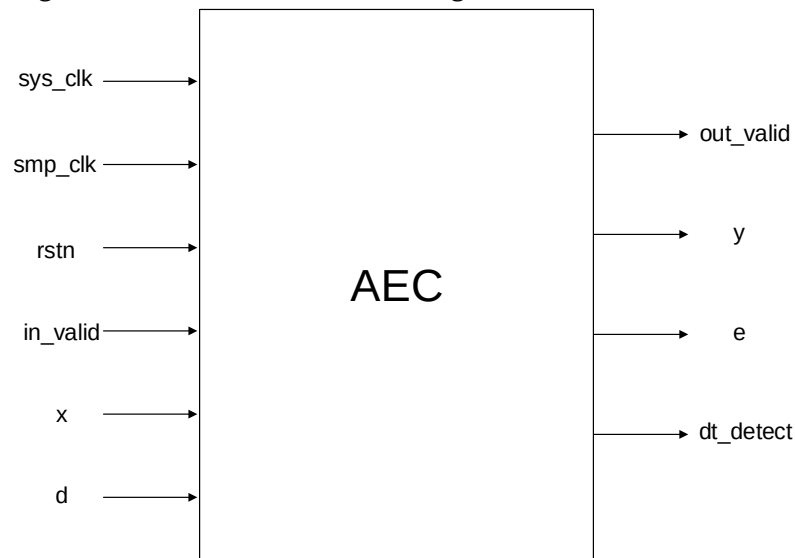
Table 3-1 Algorithm Variable List

Variable	Meaning
n	Current index
N	Filter length
x(n)	Current input sample (near-end input)
d(n)	Desired signal sample (far-end input)
X(n)	Matrix of the last two input signal vectors
w(n)	Filter coefficient vector
y(n)	Output of the adaptive filter
e(n)	Error between x(n) and d(n) (near-end output)
x _{ma}	Moving average for input signals
d _{ma}	Moving average for required signals
a	Double-talk detection smoothing coefficient
T	Double-talk detection threshold

3.3 Port Description

The IO ports of Gowin AEC IP are shown in Figure 3-2 below.

Figure 3-2 Gowin AEC IP Port Diagram



For the detailed IO ports description of Gowin AEC IP, please refer to Table 3-2.

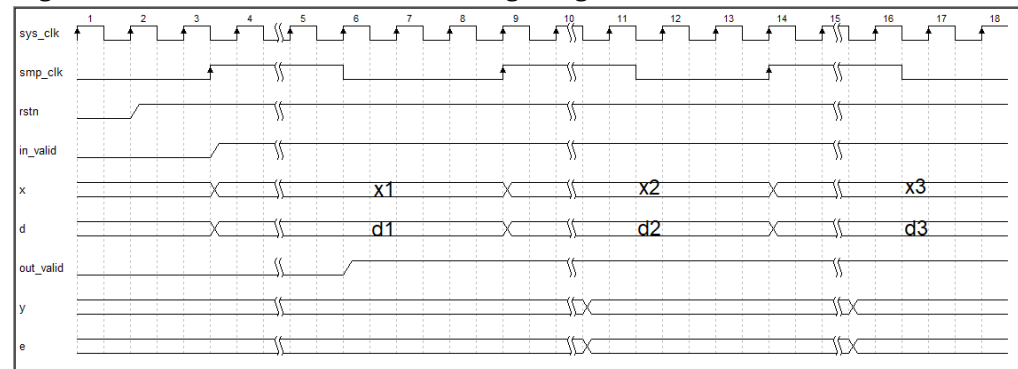
Table 3-2 Gowin AEC IP IO Description

Signal	Width	I/O	Description
sys_clk	1	Input	System clock signal
smp_clk	1	Input	Sampling clock signal
rstn	1	Input	Reset signal, active low.
in_valid	1	Input	Input data valid
x	16	Input	Near-end input signal
d	16	Input	Far-end input signal
out_valid	1	Output	Output data valid
y	16	Output	Filter output
e	16	Output	Near-end output after echo cancellation
dt_detect	1	Output	Double-talk detection output

3.4 Timing Description

The timing diagram of Gowin AEC IP is shown in Figure 3-3.

Figure 3-3 Gowin AEC IP Mode Timing Diagram



As shown in the above figure, *x* and *d* should be ready before the next rising edge of *smp_clk*, then *in_valid* is asserted to input data into Gowin AEC IP. The *out_valid* signal will be asserted before the next rising edge of *smp_clk*.

System Clock Frequency Formula

For different filter lengths (*N*), the minimum required system clock frequency is:

$$f_{sys_clk} = f_{smp_clk} \times (5N) + 200$$

The example is as follows:

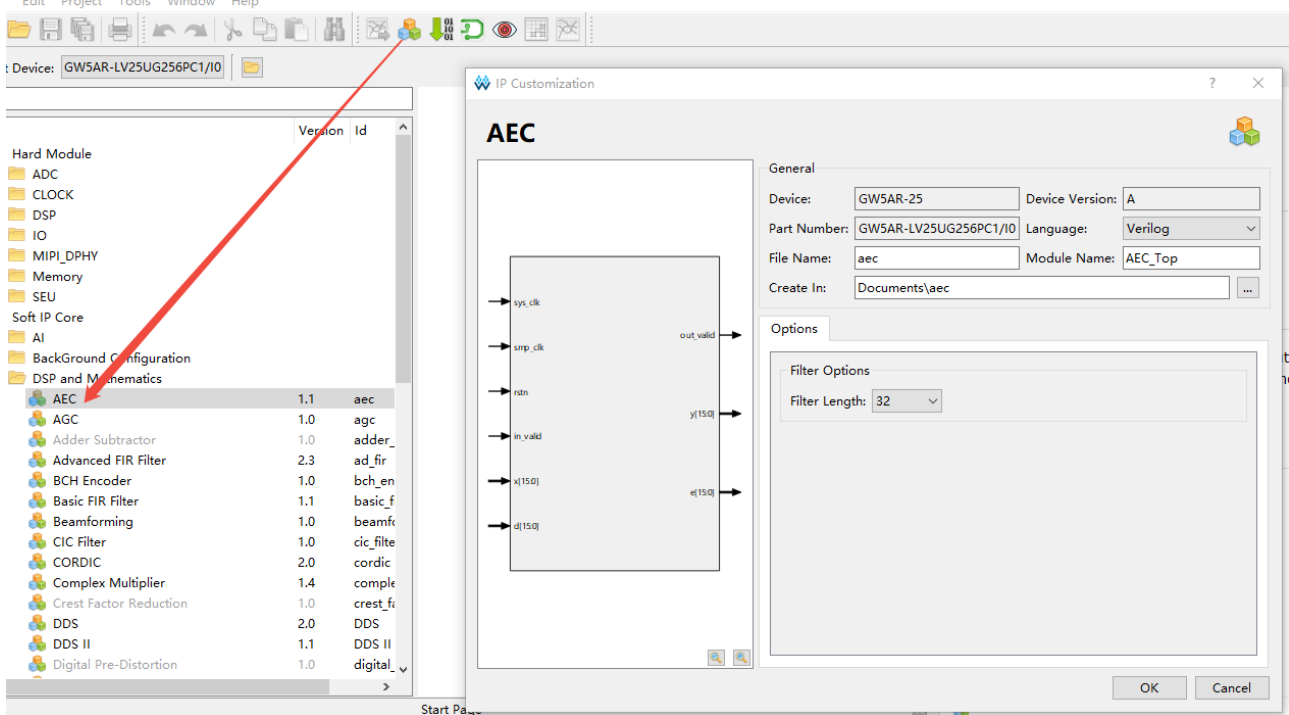
If the filter length is 512, the sampling frequency is 8 KHz.

$$f_{sys_clk} = 8000 \times 5 \times 512 + 200 = 20\text{MHz}$$

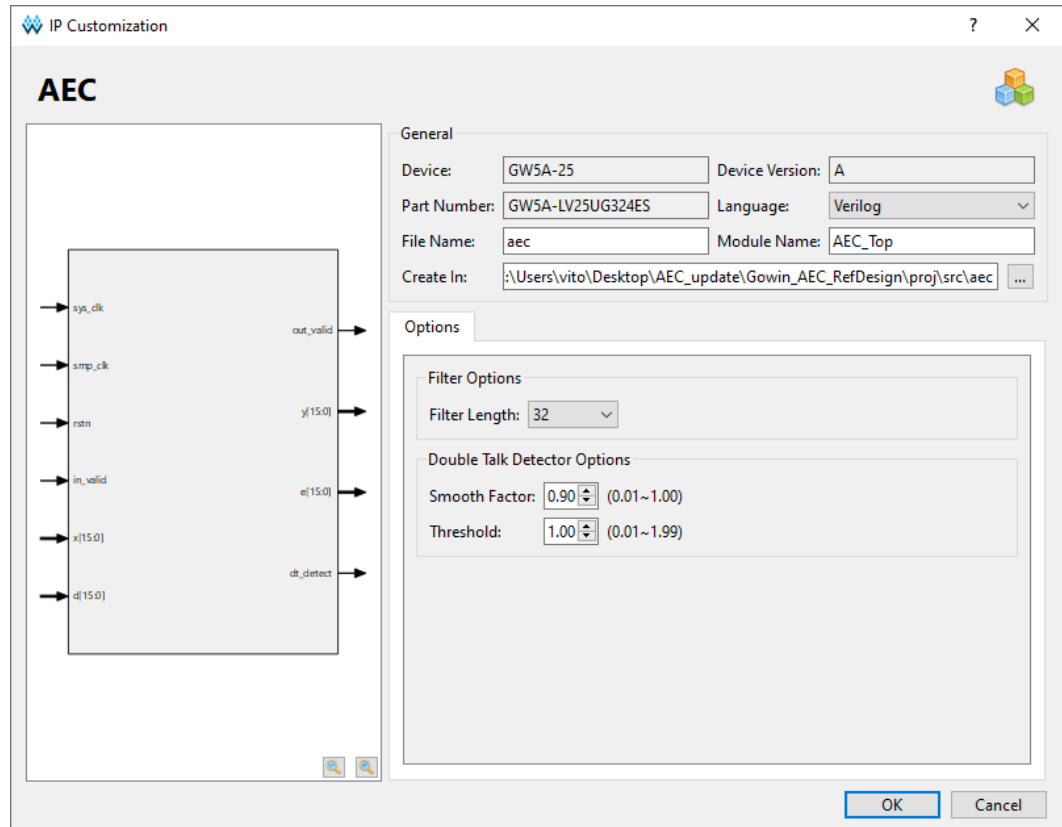
4 Interface Configuration

Start "IP Core Generator" from the "Tools" menu in Gowin Software, click "DSP and Mathematics" to call and configure "AEC" IP. Alternatively, it can also be accessed using the toolbar icon, as shown in Figure 4-1.

Figure 4-1 Open the IP Configuration Interface Via Toolbar Icon



The configuration interface of Gowin AEC IP is as shown in Figure 4-2.

Figure 4-2 Gowin AEC IP Configuration Interface

In this manual, GW5A-LV25UG324ES is used as an example.

- **Create In:** Specifies the path where the IP core folder is generated; users can modify it.
- **File Name:** Specifies the name of the generated IP file; users can modify it.
- **Module Name:** Specifies the name of the generated IP module; users can modify it.

The configuration options of Gowin AEC IP are described in the table below.

Table 4-1 Configuration Options

Option	Description
Filter Options	Filter length
Double Talk Detector Options	Smooth Factor: Ranges from 0.01 to 1.00
	Threshold: Ranges from 0.01 to 1.99

5 Reference Design

Please refer to the related test cases in [RefDesign](#).

6 File Delivery

The delivery file of Gowin AEC IP includes documentation, source code and reference design.

6.1 Document

The folder mainly contains the user guide in PDF.

Table 6-1 Document List

Name	Description
IPUG761, Gowin AEC IP User Guide	Gowin AEC IP User Guide, namely this one.

6.2 Design Source Code (Encryption)

The encrypted code folder contains the RTL encrypted code of Gowin AEC IP, which is used by the GUI to generate the required IP core in Gowin Software.

Table 6-2 AEC Design Source Code List

Name	Description
aec.v	The top-level file of the IP core, which provides you with interface information, encrypted.

6.3 Reference Design

Gowin AEC IP RefDesign folder contains the netlist file, reference design, constraints file, top-level file and the project file, etc.

Table 6-3 Gowin AEC IP RefDesign File List

Name	Description
top.v	The top module of reference design
AEC.cst	Project physical constraints file
AEC.sdc	Project timing constraints file
aec	AEC project folder
aec.v	Generates AEC IP top-level file, encrypted.
aec.vo	Generates AEC IP netlist file

