



Gowin RAM Based Shift Register IP

User Guide

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Revision History

Date	Revision	Description
12/10/2018	1.0E	Initial version released.
03/28/2019	1.1E	Supported products updated.
09/08/2023	1.2E	● GW5A, GW5AT, and GW5AST devices added. ● The descriptions of BSRAM removed.

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1 About This Guide

1.1 Purpose

Gowin RAM Based Shift Register IP User Guide include features, port descriptions, timing descriptions, configuration call and reference design, etc, used to help you quickly learn the features and usage of Gowin RAM Based Shift Register IP. The software screenshots in this manual are based on 1.9.9 Beta-3. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Product Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terms and Abbreviations

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Terms and Abbreviations

Terms and abbreviations	Full name
FIFO	First Input First Output
GSR	Global Set/Reset
IP	Intellectual Property
LUT	Look-up Table
OSC	Oscillator
RAM	Random Access Memory
REG	Register
SSRAM	Shadow Static Random Access Memory

1.4 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

URL: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Gowin RAM Based Shift Register IP Introduction

Gowin RAM Based Shift Register IP provides an efficient multi-bit width shift register that can be used as a FIFO-like data buffer or delay line function to create fixed-length and variable-length shift registers, as shown in Table 2-1.

Table 2-1 Gowin RAM Based Shift Register IP

Gowin RAM Based Shift Register	
IP core application	
Logical resource	See Table 2-3, Table 2-4, Table 2-5
Delivery document	
Designing documents	Verilog (encrypted)
Reference design	Verilog
TestBench	Verilog
Test design flow	
Integrated software	GowinSynthesis
Application software	Gowin Software (V1.9.9 Beta-3 and above)

2.2 Main Features

- Supports GW1N, GW1NR, GW2A, GW2AR, GW5A, GW5AT, GW5AST series

Note!

The 1K, 2K, 2K version B, 4K, 4K version B in GW1N series and 4K, 4K version B in GW1NR series do not support SSRAM, and the SSRAM option is grayed out when you select RAM Type.

- Can create fixed-length, lossy variable or lossless variable shift

registers.

- The speed of the variable length shift register can be optimized or the resource can be optimal.
- Design is based on LUT and SSRAM implementation.

2.3 Maximum Frequency

The maximum frequency of Gowin RAM Based Shift Register IP is determined mainly by the resources occupied and the speed grade of the devices used, as shown in Table 2-2.

Table 2-2 Gowin RAM Based Shift Register IP Maximum Frequency Example

Device series	Speed Grade	Maximum Frequency(MHz)	Note
GW2A-55	6	160	● IP settings: 8 bits, REG, Variable Shift Lossy, Max Number of Shifts = 16 ● This result is for reference only, and the specific results are subject to the actual test.
	7	179	
	8	223	
GW1N-4	4	95	
	5	115	
	6	137	

2.4 Resource Utilization

RAM-based Shift Register is implemented in Verilog language. The resources are different because of different implementations. The IP can be implemented based on LUT and SSRAM. Table 2-3, Table 2-4 and Table 2-5 are shown.

Table 2-3 Resource Utilization in Lossy Variable Shift Mode

Device Series	Speed Grade	Implementation	Device	Resource Utilization	Note
GW2A-55	8	LUT Based	LOGICS	3002	Data Width=8; MAX Number of Shifts=512; The SET and CLEAR signals are not configured.
			REG	4113	
		SSRAM Based	LOGICS	603	
			REG	18	

Table 2-4 Resource Utilization in Lossless Variable Shift Mode

Device Series	Speed Grade	Implementation	Device	Resource Utilization	Note
GW2A-55	8	LUT Based	LOGICS	2997	Data Width=8; MAX Number of Shifts=512; The SET and CLEAR signals are not configured.
			REG	4139	
		SSRAM Based	LOGICS	655	
			REG	42	

Table 2-5 Resource Utilization in Fixed Shift Mode

Device Series	Speed Grade	Implementation	Device Name	Resource Utilization	Note
GW2A-55	8	LUT Based	LOGICS	2987	Data Width=8; Number of Shifts=512; The SET and CLEAR signals are not configured.
			REG	4113	
		SSRAM Based	LOGICS	584	
			REG	18	

3 Functional Description

3.1 Gowin RAM Based Shift Register IP function

Gowin RAM Based Shift Register IP contains three shift modes:

- Fixed Shift
- Variable Shift Lossy
- Variable Shift Lossless

3.1.1 Fixed Shift

In the fixed shift mode, the input data is shifted by the corresponding shift value (Number of Shifts) and output. The shift value ranges from 2 to 1024.

3.1.2 Variable Shift Lossy

The shift length of the lossy variable shift mode is controlled by the input of "ADDR", and the input data is delayed after "ADDR+1" cycles.

When the "ADDR" changes, the output data is invalid within a certain clock period. See the timing description in Section 5 for details.

Note!

ADDR ranges from 1 to Max Number of Shifts.

3.1.3 Variable Shift Lossless

The shift length of the lossless variable shift mode is controlled by the input of "ADDR", and the input data is delayed after "ADDR+1" cycles.

When the "ADDR" changes, the output data will repeat the previous delay data in a certain clock cycle. For details, see the timing description in Section 5. Please use it as needed.

Note!

ADDR ranges from 0 to Max Number of Shifts.

3.1.4 SSET/SCLR

- When the SET option is selected, the SSET input port is generated. Set to 1 when SSET is active.
- Check the CLEAR option to generate the SCLR input port, and set to 0 when SCLR is active.
- When both SET and CLEAR are checked, and both are valid, SSET has a higher priority than SCLR and is set to 1.

4 Port Description

Gowin RAM Based Shift Register IP Port

Details on the IO port of the Gowin RAM Based Shift Register IP are shown in Table 4-1.

Table 4-1 Gowin RAM Based Shift Register IP IO Port

Name	I/O	Bit width	Comment
clk	Input	1	Clock
Reset	Input	1	Reset signal, active-high
Din	Input	Variable	Input data; the bit width is [DSIZE-1:0]
ADDR	Input	Variable	Length of Latency in Variable Shift Lossy/Variable Shift Lossless mode; the bit width is varied according to the maximum shift length
SSET	Input	1	Output port is set; this pin exists when the SET option is checked
SCLR	Input	1	Output port reset; this pin exists when the CLEAR option is checked
Q	Output	Variable	Output Data; the bit width is [DSIZE-1:0]

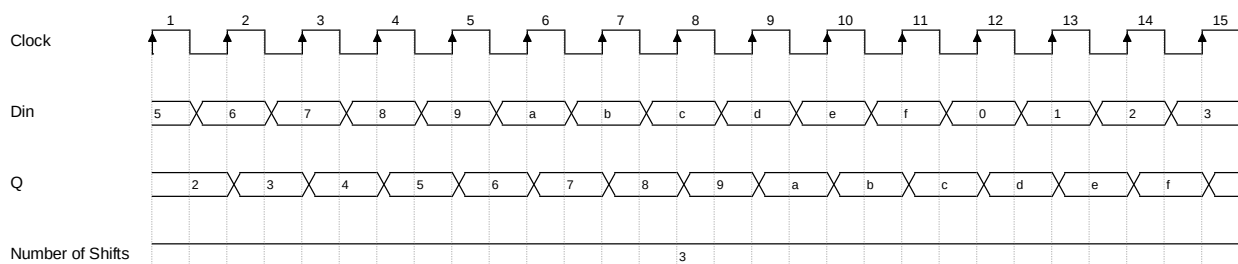
5 Timing Description

This chapter is intended to introduce the timing of input signals in various modes of Gowin RAM Based Shift Register IP.

5.1 Fixed Shift Timing

The timing of the fixed shift mode is shown in Figure 5-1.

Figure 5-1 Timing Diagram of Fixed Shift Mode (ADDR=3)



5.2 Lossy Variable Shift Timing

The timing of the lossy variable shift mode is shown in Figure 5-2 and Figure 5-3.

**Figure 5-2 ADDR Stable Timing Diagram of Lossy Variable Shift Mode
(ADDR=3)**

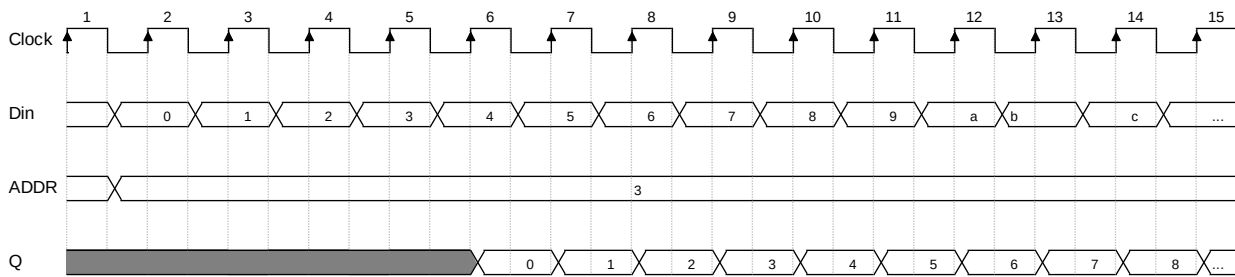
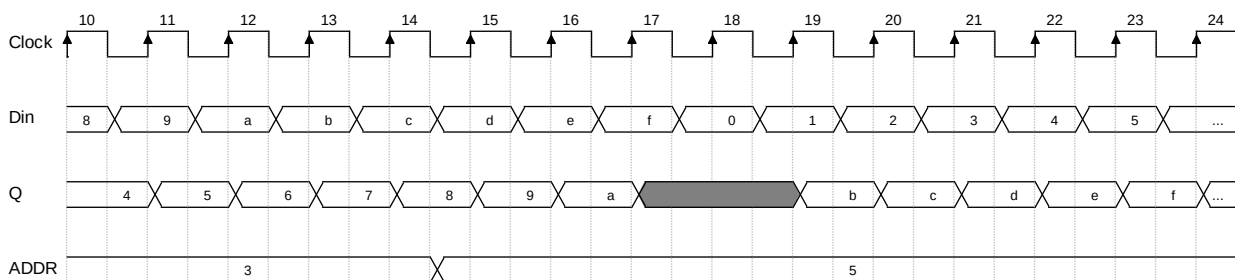
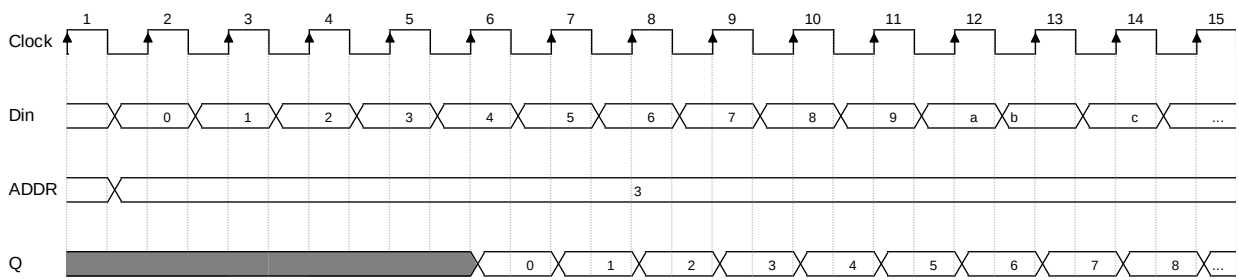
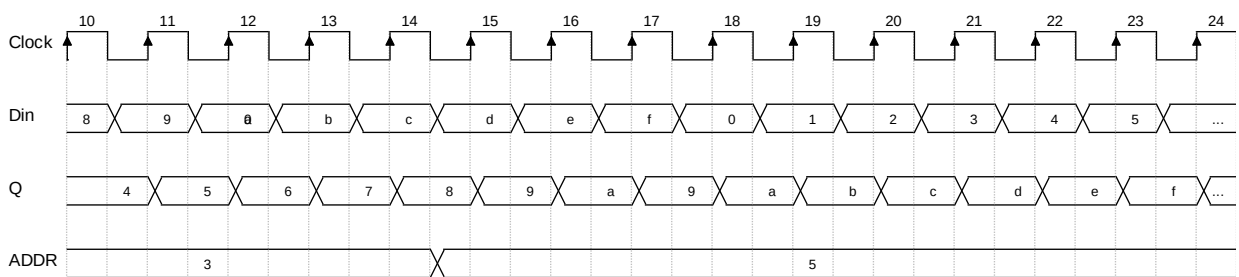


**Figure 5-3 ADDR Change Timing Diagram of Lossy Variable Shift Mode
(ADDR Changes from 3 to 5)**



5.3 The Timing of the Lossless Variable Shift Mode

The timing of the lossless variable shift mode is shown in Figure 5-4 and Figure 5-5.

Figure 5-4 ADDR Stable Timing Diagram of Lossless Variable Shift (ADDR=3)**Figure 5-5 ADDR Change Timing Diagram of Lossless Variable Shift Mode (ADDR Changes from 3 to 5)**

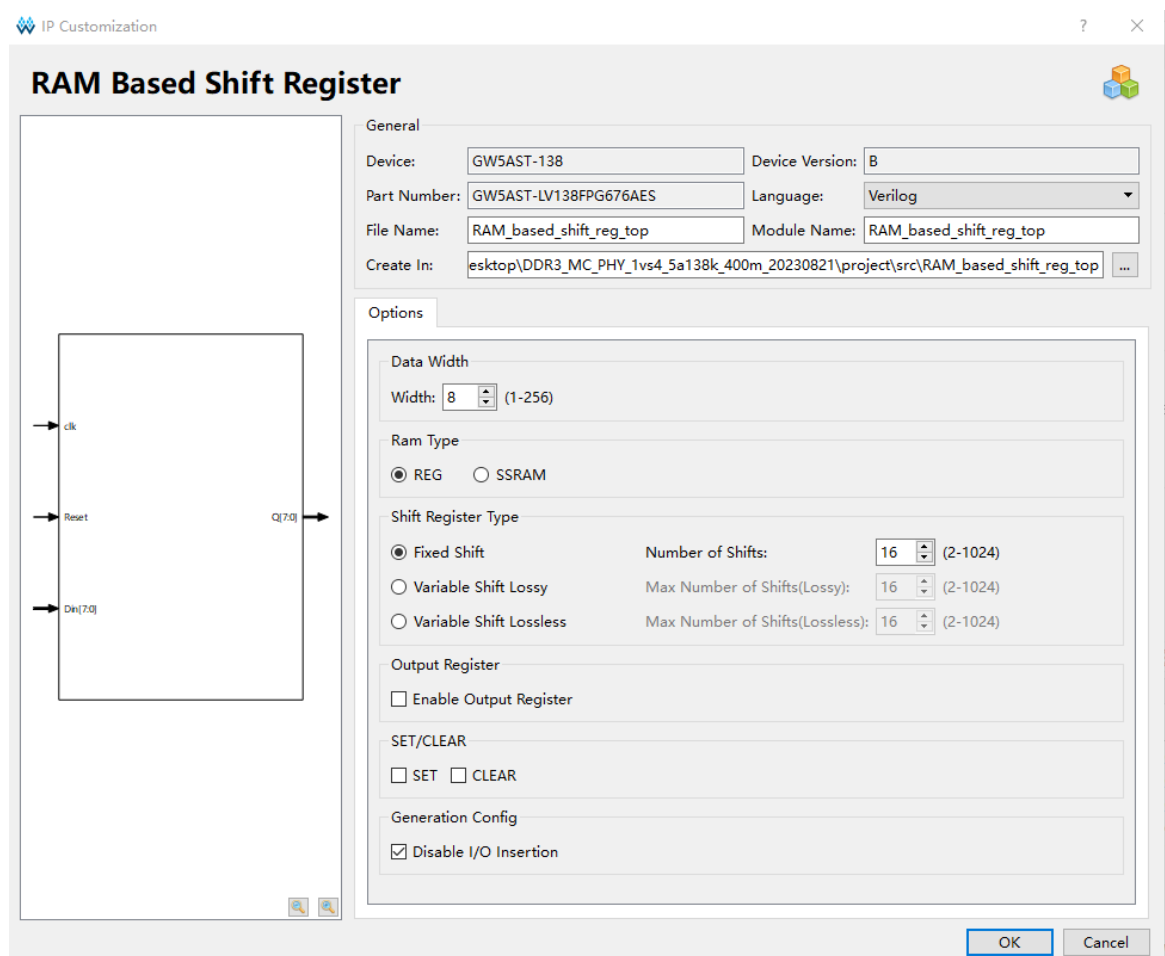
6 Configuration and Call

Click "Tools > IP Core Generator" in Gowin Software to open IP Core Generator to complete the call and configure RAM Based Shift Register IP

6.1 RAM Based Shift Register Configuration Interface

The RAM Based Shift Register configuration interface is shown in Figure 6-1.

Figure 6-1 RAM Based Shift Register Configuration Interface



1. You can modify the address of the RAM Based Shift Register generated file by "Create In".
2. The generated RAM Based Shift Register top-level module name can be configured by "Module Name".
3. The name of the RAM Based Shift Register file can be configured by "File Name".
4. You can configure Data Width, RAM Type, Shift Register Type, etc. in "Options".
5. By default, Data Width=8; RAM Type is REG; Type is Fixed Shift (Number of Shifts is 16); Enable Output Register, SET and CLEAR are not checked.

6.2 RAM Based Shift Register Options Configuration

The RAM Based Shift Register Options configuration are shown in Table 6-1.

Table 6-1 RAM Based Shift Register Options Configuration

Option		Description
Data Width		1~256
Ram Type	LUT Based	Based on LUT
	SSRAM Based	Based on SSRAM; when Device is GW1N-1/GW1N-2/GW1N-4, SSRAM Based can not be selected.
Shift Register Type		Fixed shift
		Variable shift lossy
		Variable shift lossless
Output Register		The specified register is used to output data, which causes the output to generate an additional clock cycle delay.
SET/CLEAR		When the SET is configured, the SSET input port is generated. When SSET is valid, it is set to 1, and the SSET priority is higher than SCLR.
		When CLEAR is configured, the SCLR input port is generated. When SCLR is valid, it is set to 0, and the SCLR priority is lower than SSET.

