



Gowin FD Adaptive Filter User Guide

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Revision History

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1 About This Guide

1.1 Purpose

Gowin FD Adaptive Filter User Guide provides a description of the function, feature, port, timing, configuration call, and reference design, etc. The guide helps users to quickly learn the feature and usage of Gowin FD Adaptive Filter IP.

1.2 Supported Products

The information presented in this guide applies to the following products:

1. GW1N-6, GW1N-9
2. GW1NR-9
3. GW2A series of FPGA Products
4. GW2AR series of FPGA Products

1.3 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series FPGA Products Data Sheet
2. GW1NR series FPGA Products Data Sheet
3. GW2A series FPGA Products Data Sheet
4. GW2AR series FPGA Products Data Sheet
5. Gowin YunYuan Software User Guide

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in

the Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Terminology and Abbreviations	Full Name
LMS	Least Mean Square
FIR	Finite Impulse Response
RAM	Random Access Memory
FD Adaptive Filter	Frequency Domain Adaptive Filter
FFT	Fast Fourier Transform
DSP	Digital Signal Processing
ALU	Arithmetic Logic Unit
LUT	Look-up Table
REG	Register
BSRAM	Block Static Random Access Memory
SSRAM	Shadow Static Random Access Memory
GSR	Global Set/Reset

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

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2Overview

2.1 Gowin FD Adaptive Filter IP Introduction

Gowin FD Adaptive Filter IP uses fast block least mean square (LMS) to implement FIR filter in the frequency domain, as shown in the Table 2-1.

Table 2-1 Gowin FD Adaptive Filter IP

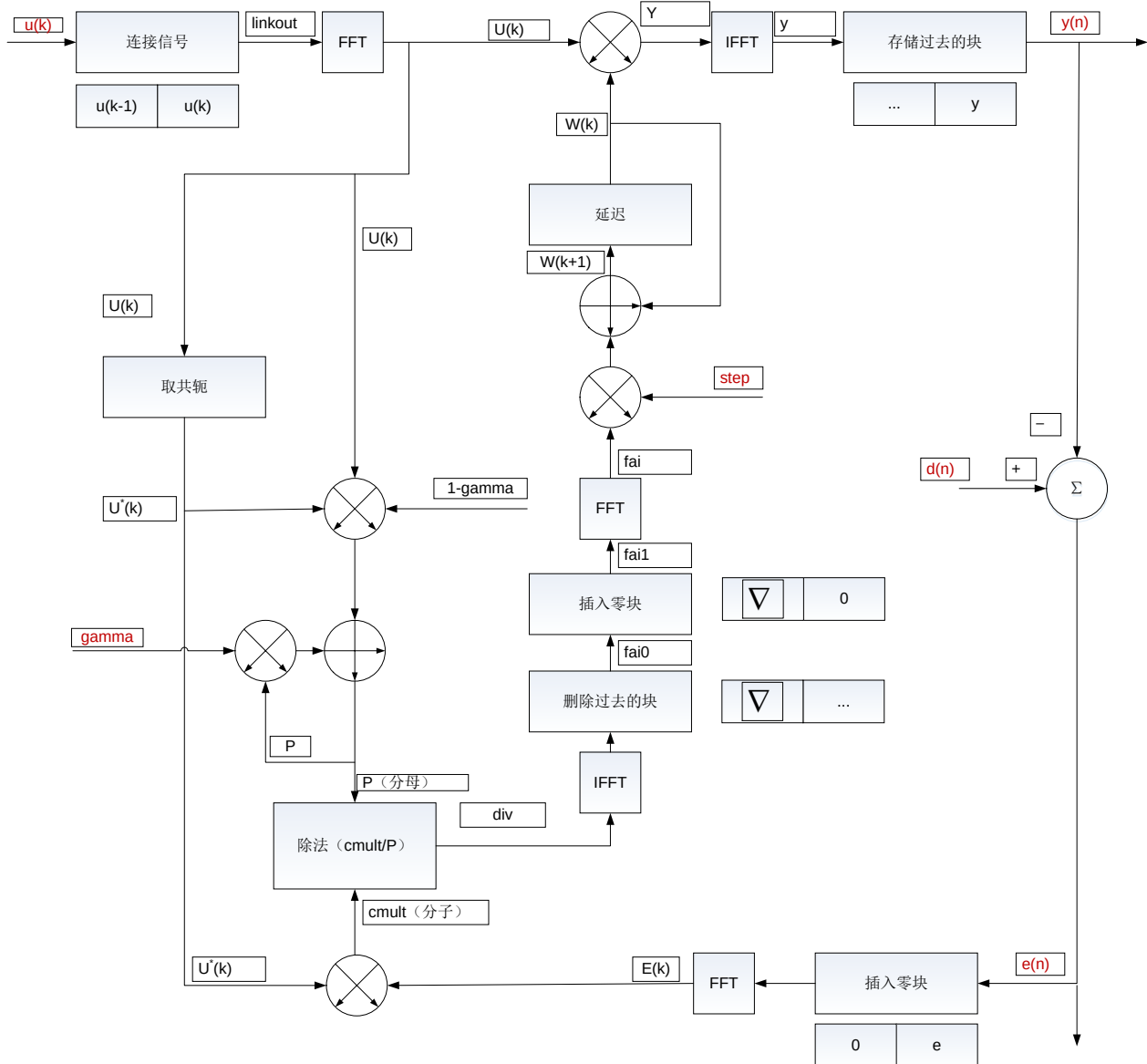
Gowin FD Adaptive Filter	
IP Core Application	
Supported Devices	GW1N-6, GW1N-9 GW1NR-9 GW2A series GW2AR series
Logic Resource	See Table 3-1
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GowinYunYuan

2.2 Introduction to Gowin FD Adaptive Filter Algorithm

Gowin FD Adaptive Filter Algorithm, that is, the Frequency Domain Adaptive Filter Algorithm, uses fast block least mean square (LMS) to implement FIR filter in the frequency domain. It can automatically adjust its parameters to meet the requirements of the optimal criterion function when the statistical characteristics of the input process change or are unknown; Through FFT transformation, linear convolution and linear correlation can be realized quickly, and the time domain signal operation can be turned into the frequency domain signal operation, and the convolution operation can be turned into multiplication operation.

The algorithm implementation diagram is shown in Figure 2-1 as below. Where the $u(k)$ and $d(n)$ are the input of a calculation, the $y(n)$ and $e(n)$ are the output. Step (0.1) is the step length of adaptive calculation; Gamma (0.9) is the forgetting factor.

Figure 2-1 Algorithm Implementation Diagram



3Feature and Performance

3.1 Key Feature

The input sequence length (512/1024/2048/4096) can be configured.

3.2 Max. Frequency

The maximum frequency of Gowin FD Adaptive Filter IP is mainly determined by the occupied resources and the speed grade of the devices. Take gw2a-55 and input sequence length 1024 as an example. The maximum frequency can reach 80M.

3.3 Latency

Gowin FD Adaptive Filter IP latency refers to the time latency between data input and data output.

Gowin FD Adaptive Filter IP configures different input sequence lengths with inconsistent latency between input and output.

3.4 Resource Utilization

The FD Adaptive Filter is realized by Verilog language. At present, the Gowin FPGA family enjoys a universal structure, so the resource amount of different series of FPGA chips to achieve this project is basically the same. However, due to the different IP configuration, its resource utilization may be different.

Take gw2a-55 and input sequence length 1024 as an example. The actual resource utilization is shown in the Table 3-1

Table 3-1 FD Adaptive Filter Resource Utilization

Device	Name	Resource Utilization	Remarks
GW2A-LV55PG484C8/I7	LUT	4280	—
	ALU	725	
	REG	3713	
	BSRAM	21	
	SSRAM	104	
	DSP Macros	9	

4Function Description

4.1 FD Adaptive Filter Function

Users can configure the length of the input sequence (512/1024/2048/4096) to implement the FD Adaptive Filter algorithm with different length sequences. The algorithm gets the result by looping block calculation. The looping calculation needs a certain number of times while calculating. When the input sequence is 512 points, the initial convergence result can be obtained. The better convergence result can appear when the sequence reaches 1024 points or longer.

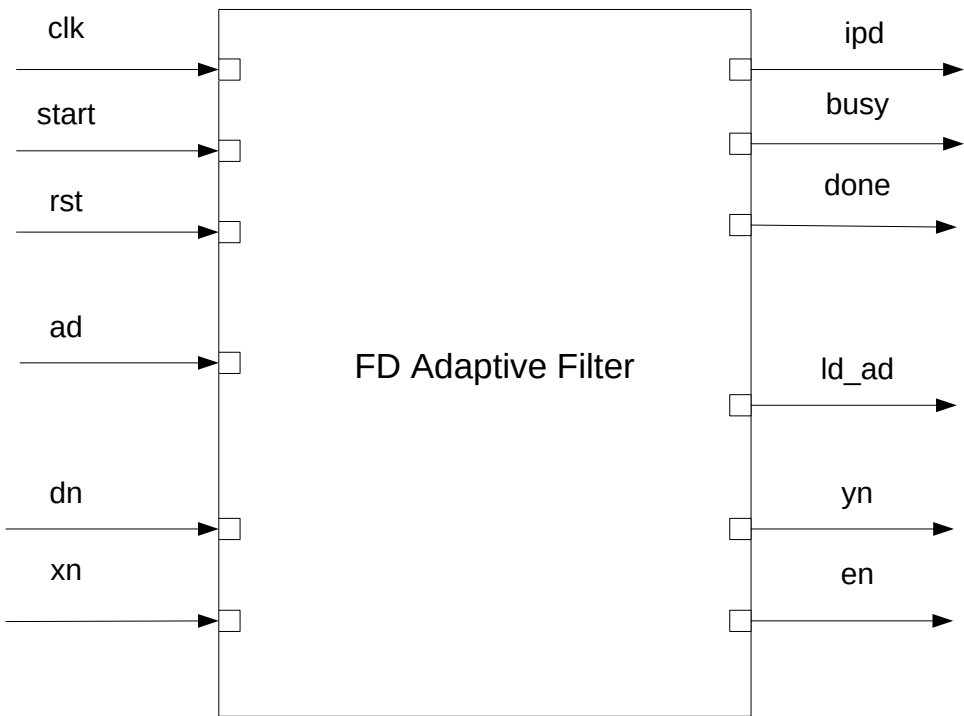
The commonly used sequence length is 1024 points. When a longer sequence is used, the timing sequence can be appropriately configured and extended by 1024, which can reduce the resource utilization and satisfy the basic use. Similarly, other lengths can also be extended.

5Port Description

5.1 Gowin FD Adaptive Filter IP Port

Gowin FD Adaptive Filter IP I/O Port is shown in Figure 5-1.

Figure 5-1 Gowin FD Adaptive Filter IP Port Figure



The I/O port details for Gowin FD Adaptive Filter IP are shown inTable 5-1 below.

Table 5-1 Gowin FD Adaptive Filter IP I/O Port

Name	I/O	Data Width	Note
clk	Input	1	Clock
rst	Input	1	Reset signal, active-high.
start	Input	1	Start signal, active-high.
ad	Input	Changeable	The sequence position of the next output data when the data is unloaded; The bit width depends on the length of the input sequence
dn	Input	[17:0]	Desired signal input;
xn	Input	[17:0]	Actual signal input;
ipd	Output	1	Indication of data inputting , active-high, indicate data is inputting
busy	Output	1	Indication of algorithm calculation, active-high, indicate the algorithm is in progress
done	Output	1	Indication of algorithm completion, active-high, indicate the algorithm has been completed and the data can be unloaded.
ld_ad	Output	Changeable	When loading data, indicate the sequence position of the next trigger along the data to be loaded; The bit width depends on the length of the input sequence
en	Output	[17:0]	Error signal output
yn	Output	[17:0]	Estimated signal output

6Timing Description

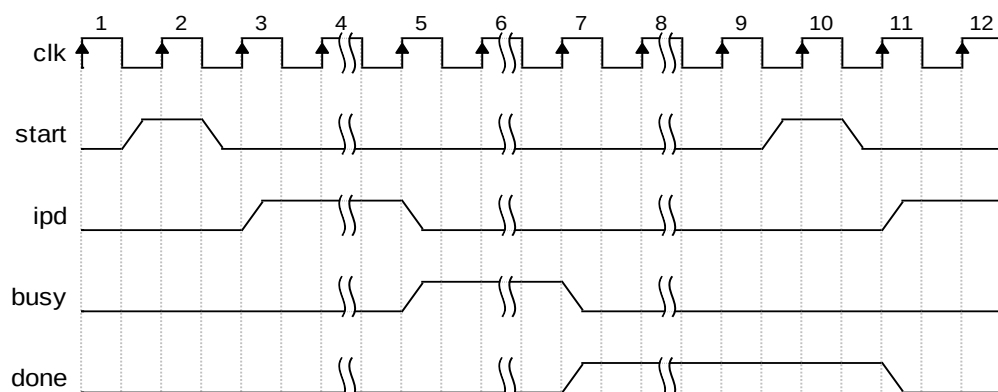
This section aims to introduce the timing of Gowin FD Adaptive Filter IP.

6.1 State sequence

Gowin FD Adaptive Filter IP state sequence is shown in the figure 6-1.

Ipdc signal is pulled up and maintained in the next period when CLK recognizes start=1, indicating that data is inputting. After finished, the ipdc signal is pulled down. At the same time, the busy signal is pulled up, indicating that the algorithm is running. After finished, the busy signal is pulled down, while the done signal is pulled up, indicating that the operation has been completed and the data can be unloaded

Figure 6-1 FD Adaptive Filter State Sequence



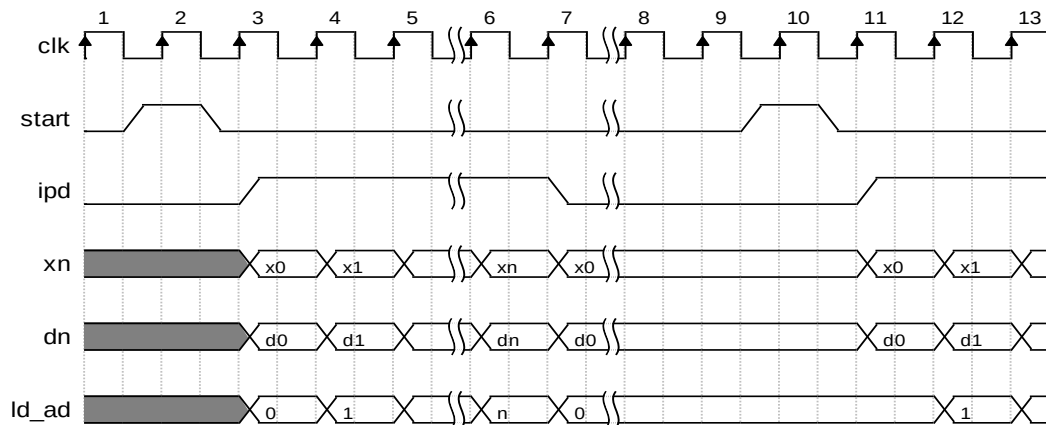
6.2 Input data Sequence

Gowin FD Adaptive Filter IP input data sequence is shown in the figure 6-2.

When ipdc=1, indicate the data is inputting, and Id_ad indicates the

sequence position of the next trigger along the data to be loaded;

Figure 6-2 Gowin FD Adaptive Filter IP Input data Sequence Figure

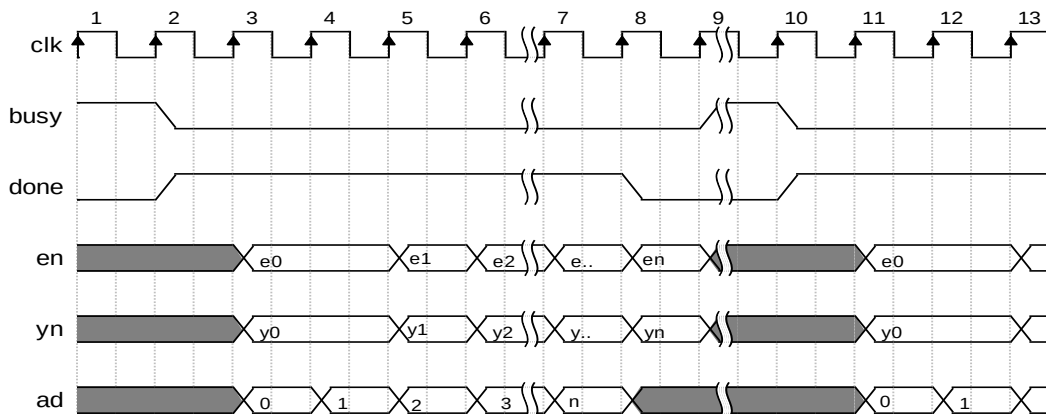


6.3 Output data Sequence

Gowin FD Adaptive Filter IP output data sequence is shown in the figure 6-3.

When done =1, it means that the data can be output. When the user inputs AD, the data of this position will be output in the next period.

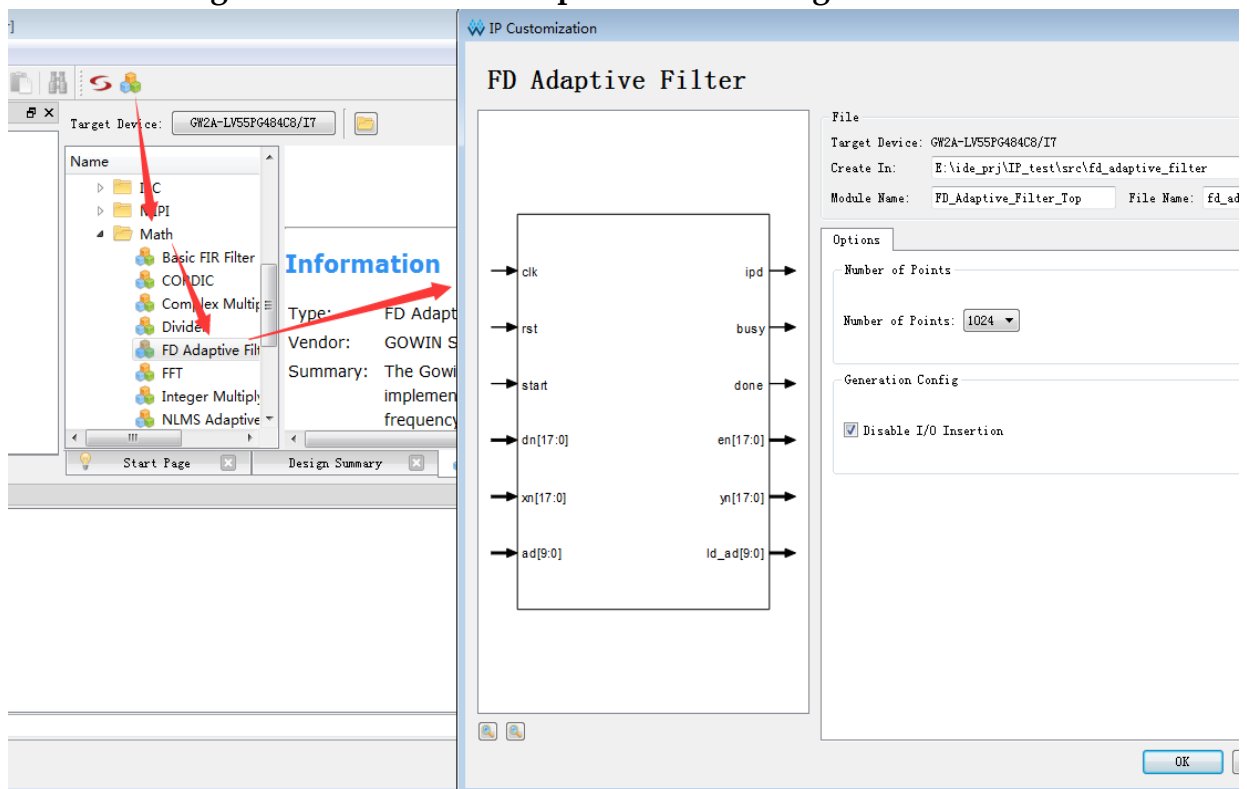
Figure 6-3 Gowin FD Adaptive Filter IP Output Data Sequence Figure



7 Configuration and Call

Start "IP Core Generator" from the "Tools" menu in the Gowin YunYuan software, then complete the call and configure FD Adaptive Filter IP. Toolbar icon is also available as shown in Figure 7-1.

Figure 7-1 Toolbar Icon Opens the IP Configuration Interface

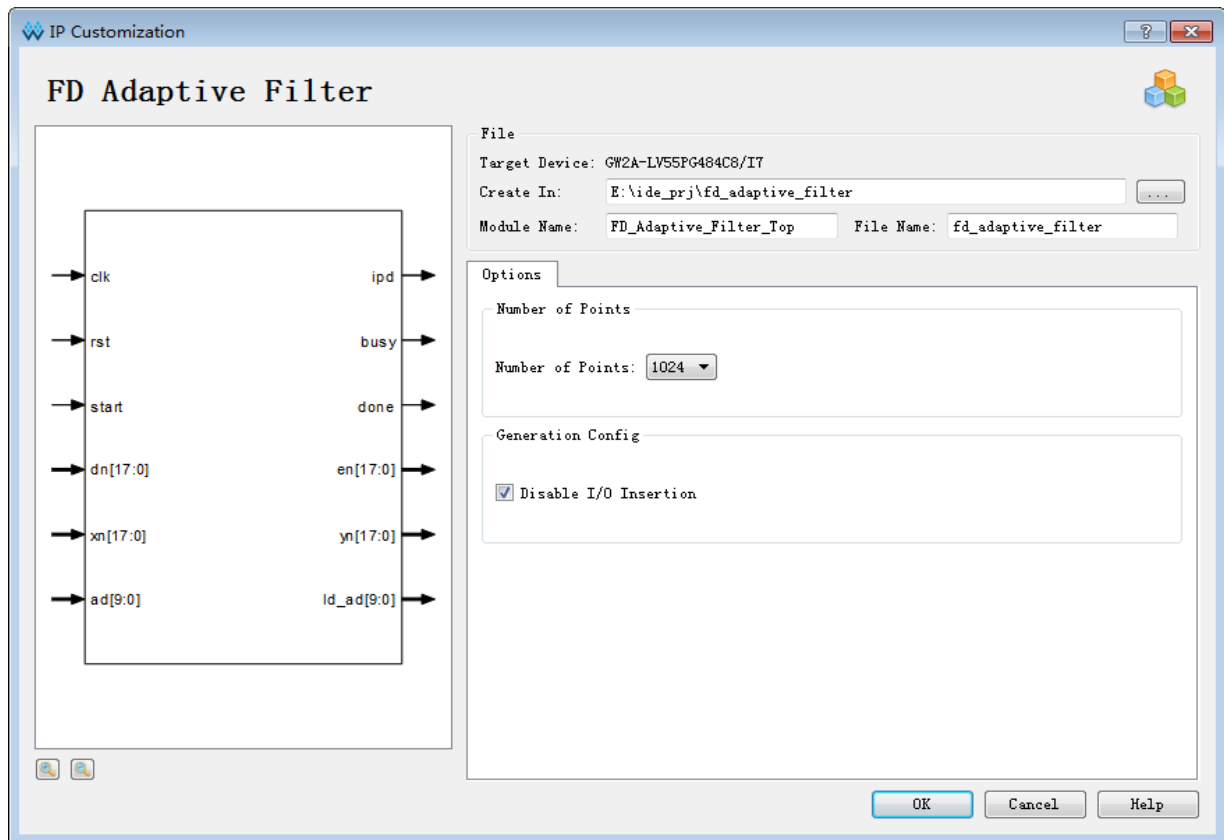


7.1 FD Adaptive Filter Configuration

7.1.1 FD Adaptive Filter Configuration Interface

FD Adaptive Filter configuration interface is shown in Figure 7-2.

Figure 7-2 FD Adaptive Filter Configuration Interface



1. File Name: The File Name can be modified to generate the Name of FD Adaptive Filter IP folder.
2. Module Name: The Module Name can be modified to generate the top-level Module Name of Adaptive Filter IP.
3. Number of Points: The input sequence length can be configured by configuring Number of Points in the Options.

7.1.2 FD Adaptive Filter Options Configuration

FD Adaptive Filter options configuration is shown in Table 7-1.

Table 7-1 FD Adaptive Filter Options Options Configuration

Options	Description
Number of Points	The length of the input sequence

