



Gowin Complex Multiplier

Release Notes

RN521-1.0E, 2018-12-17

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Revision

Date	Revision	Description
2018/12/17	1.0E	● IP Core Generator supports Complex Multiplier; ● Complex Multiplier reference design release; ● User manual is released.

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1 About This Release

This release includes the Gowin Complex Multiplier IP User Guide and reference design.

The user guide and reference design of the Gowin Complex Multiplier IP can be downloaded from Gowin's official website. Among them, the reference design has been configured with specific parameters, which can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

2Overview

Gowin Complex Multiplier IP is used for multiplication of complex numbers.

Table 2-1 Gowin Complex Multiplier IP Overview

Gowin Complex Multiplier IP	
IP core application	
Chip supported	Does not support GW1N-1, GW1NS-2, GW1NS-2C All other chips support
Delivery document	
Designing documents	Verilog (encrypted)
Reference design	Verilog
TestBench	Verilog
Test design flow	
Integrated software	Synplify_Pro
Application	GoWinYunYuan

3Document

The released IP manuals are listed in the table below. You can download the PDF manuals at Gowin website or read online.

Table 3-1 Gowin Complex Multiplier IP Document

Document	Use
Gowin Complex Multiplier IP user guide.pdf	PDF

4IP Support

Because the user design and the highest frequency requirements are different, the reference design does not have associated FPGA-specific location (.cst) and timing constraints (.sdc), and the user can determine it as needed.

For customized IP design and support, please contact the Gowin Sales and Support Hotline.

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