



Gowin Complex Multiplier IP

User Guide

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Revision History

Date	Revision	Description
12/17/2018	1.0E	Initial version released.
07/04/2025	1.1E	● Section 1.2 Related Documents updated. ● Section 3.2Maximum Frequency updated. ● Section 3.3 Latency updated. ● Section 3.4Resource Utilization updated. ● IP features updated. ● Gowin Complex Multiplier IP port diagram and interface screenshots updated.

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1 About This Guide

1.1 Purpose

Gowin Complex Multiplier IP User Guide provides functional features, port descriptions, timing information, configuration, and reference designs, etc. It is intended to help users quickly understand the features and usage of Gowin Complex Multiplier IP. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.11.02. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER Series of SecureFPGA Products Datasheet](#)
- [DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X &9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)

- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terms and Abbreviations

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Terms and Abbreviations

Abbreviations and Terminologies	Meaning
DSP	Digital Signal Processing
IP	Intellectual Property
LUT	Look-up Table
RAM	Random Access Memory

1.4 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2Overview

2.1 Complex Multiplier IP Introduction

Gowin Complex Multiplier IP is designed to perform complex multiplication.

Table 2-1 Complex Multiplier IP Overview

Complex Multiplier IP	
Logical resource	Please refer to Table 3-2 and Table 3-3
Delivery document	
Designing documents	Verilog (encrypted)
Reference design	Verilog
TestBench	Verilog
Test design flow	
Integrated software	GowinSynthesis
Application	Gowin Software

Note !

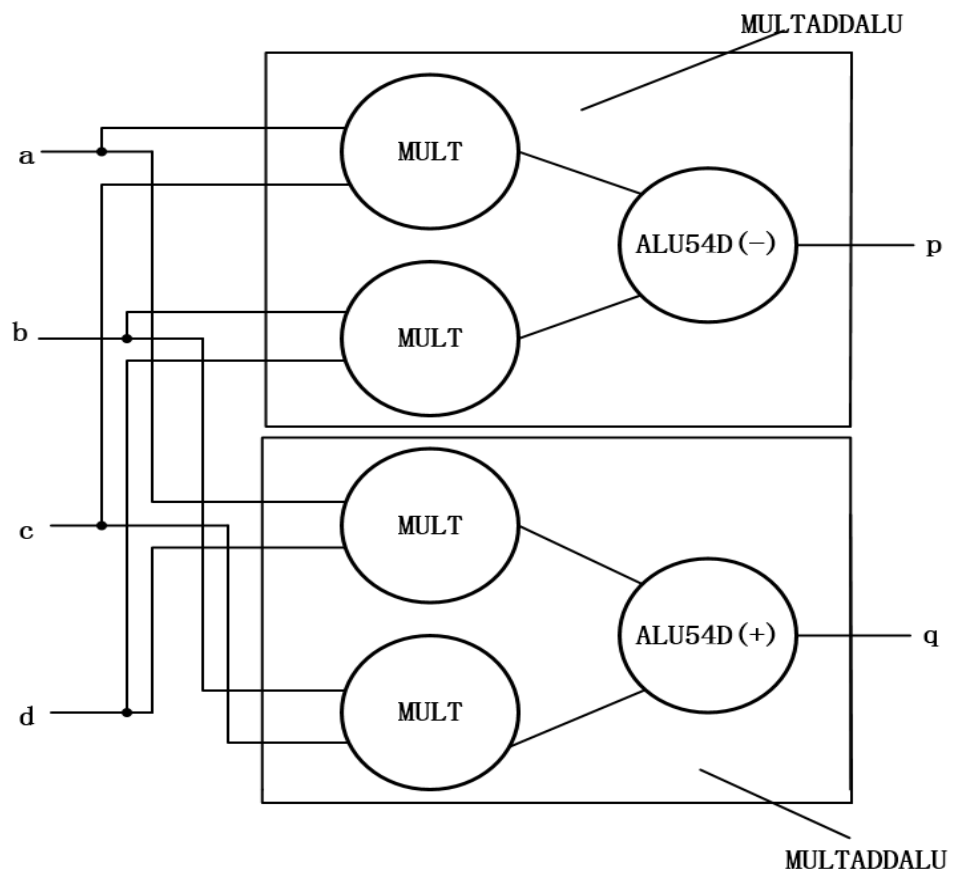
For the devices supported, you can click [here](#) to get the information.

2.2 Introduction to Complex Multiplier

Complex Multiplier is used to implement complex multiplication. The structure diagram is shown in Figure 2-1.

Gowin complex multiplier IP can be implemented by calling the multiplier (multiplier + adder).

Figure 2-1 Schematic Diagram of the Complex Multiplier Structure



3 Features and Performance

3.1 Feature

- Input data width range: 2 to 36 bits
- Supports signed input data
- Supports 3-multiply or 4-multiply algorithm
- Configurable output delay with a maximum of 2 clock cycles

3.2 Maximum Frequency

The maximum frequency of Gowin Complex Multiplier IP is determined by the speed grade of the devices and parameter configuration.

3.3 Latency

Latency in Gowin Complex Multiplier IP refers to the clock cycle delay between input and output. This latency is configurable via data registers, with a current maximum of 2 clock cycles and a minimum of zero delay.

3.4 Resource Utilization

Gowin Complex Multiplier IP can be implemented by Verilog language. Performance and resource utilization may vary depending on the density, speed, and grade of the device being used.

Take Gowin GW5A-25 series of FPGA as an example. The resource utilization of Gowin Complex Multiplier IP is shown in Table 3-1. For application verification on other Gowin FPGAs, please pay attention to the future release updates.

Gowin Complex Multiplier IP resource utilization depending on the

configuration options on the GUI.

Table 3-1 Gowin Complex Multiplier IP Resources Utilization

PN (Speed Grade)		25 (ES)	25 (ES)	25 (ES)
Resources Utilization	Data width N, multiplication algorithm	$N \leq 12$, 4-multiply algorithm	$12 < N \leq 27$, 3-multiply algorithm	$27 < N \leq 36$, 3-multiply algorithm
	BSRAM	0	0	0
	DSP	2	3	6
	REG	0	110	146
	ALU	0	194	365
	LUT	1	1	1

4 Functional Description

Users can implement complex multiplication using Gowin Complex Multiplier IP. This IP is based on a multiply-accumulate (MAC) structure to perform complex multiplication. The input data width is configurable, and different widths will result in varying hardware resource consumption. Therefore, to optimize resource utilization, users are advised to choose the smallest possible data width that still meets their design requirements.

Configuration options for Gowin Complex Multiplier IP are described below:

- Input Data Width

The input data width N can be configured through the GUI. Currently, the maximum supported bit width for signed input data is 36 bits.

- Output Data Width

When the input data width is configured as N through the GUI, the corresponding output data width will be $2N + 1$.

- Multiplication Algorithm

Users can choose between 3-multiply and 4-multiply algorithms. In general, for GW5A series of devices with $N < 12$, or GW2A/1N series of devices with $N < 18$, using the 4-multiply algorithm typically saves DSP resources and provides better timing performance. Outside of these conditions, the 3-multiply algorithm tends to save more DSP resources but consumes more logic resources, while the 4-multiply algorithm uses more DSP resources but less logic.

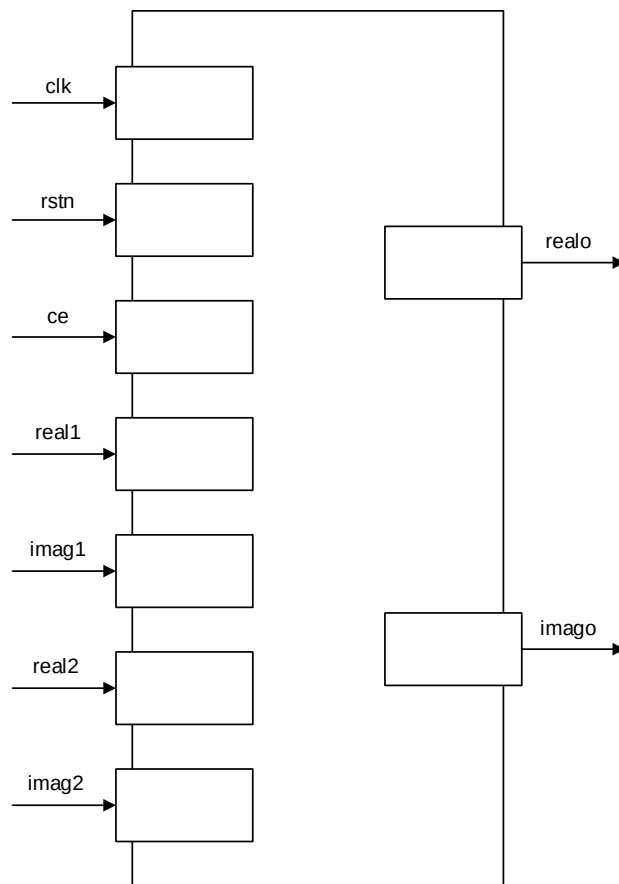
- Latency Configuration

The output delay can be configured for up to 2 clock cycles, with the minimum being zero delay.

5 Port Description

Gowin Complex Multiplier IP I/O port diagram is shown in Figure 5-1.

Figure 5-1 Complex Multiplier I/O Port Diagram



The I/O port description of Gowin Complex Multiplier IP is shown in Table 5-1.

Table 5-1 IO List of Gowin Complex Multiplier IP

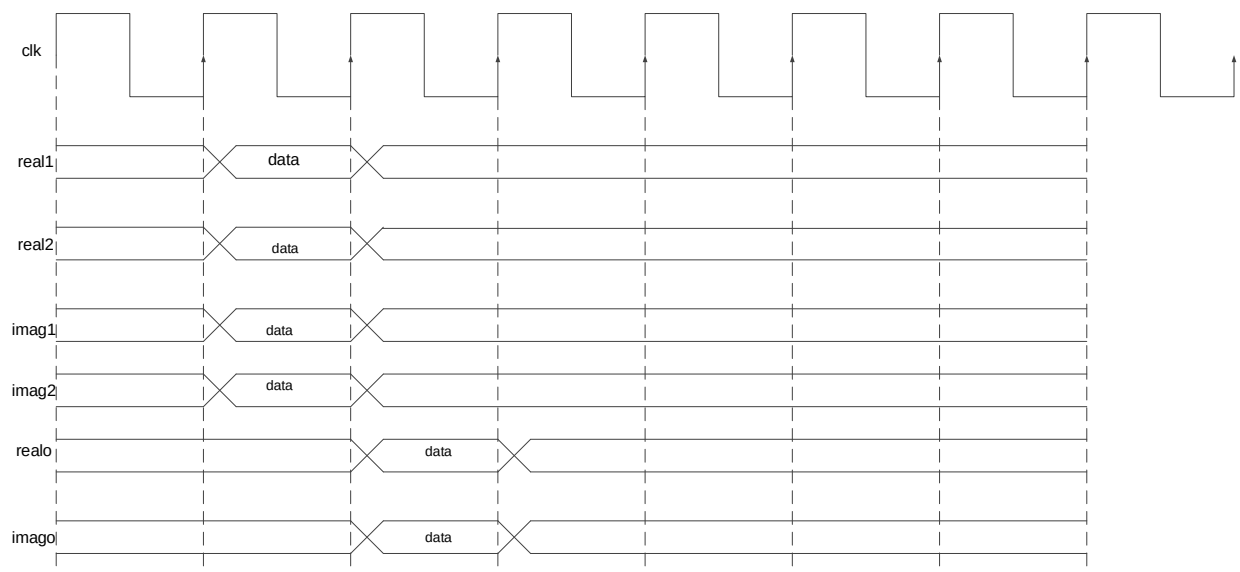
Signal	Direction	Description
clk	input	Clock signal
rstn	input	Reset signal, active-low.
ce	input	Clock enable signal
real1	input	Real input 1
real2	input	Real input 2
imag1	input	Imaginary input 1
imag2	input	Imaginary input 2
realo	output	Real output
imago	output	Imaginary output

6 Timing Description

This section is intended to introduce the output signal timing of Gowin Complex Multiplier IP.

We can achieve the purpose of output delay by passing the data through the register. The schematic diagram of the output delay for one cycle is shown in Figure 6-1.

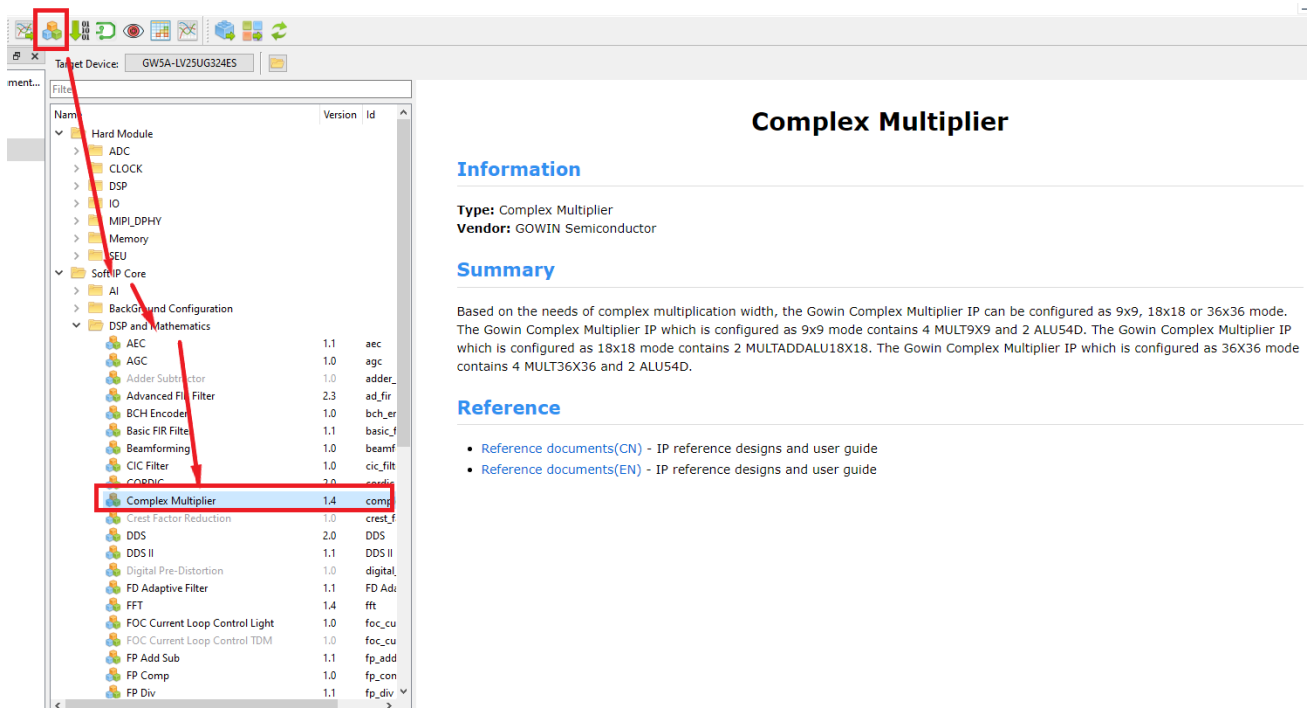
Figure 6-1 Complex Multiplier Delays One Clock Cycle of Signal



7 GUI

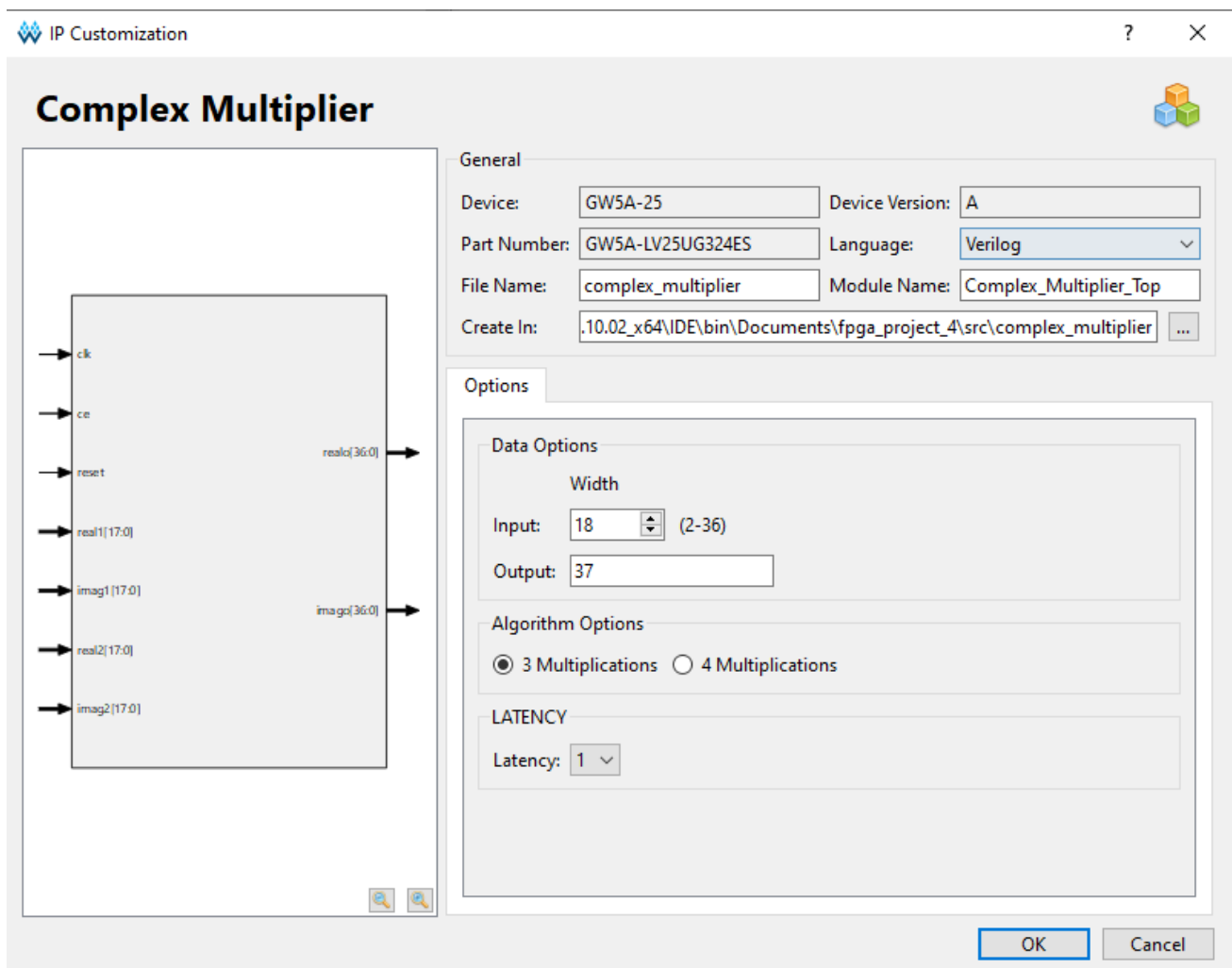
1. In Gowin Software, the "IP Core Generator" tool can be launched from the "Tools" menu to call and configure Complex Multiplier IP. After creating a project, click "IP Core Generator > Soft IP Core > Math > Complex Multiplier" to launch the Complex Multiplier, as shown in Figure 7-1.

Figure 7-1 Call Complex Multiplier



2. Complex Multiplier configuration interface is as shown in Figure 7-2.

Figure 7-2 Complex Multiplier Configuration Interface



The parameter configuration descriptions on the GUI are as follows:

- Data Options: Used to select input data width (2–36); output data width (read-only).
- Algorithm Options: You can select "3 Multiplication" and "4 Multiplication".
- LATENCY: Output latency (0–2).

8 Reference Design

This section focuses on the construction and usage of reference design examples for Complex Multiplier. The Complex Multiplier design example consists of a single module. See the [Complex Multiplier](#) reference design for details.

In the design example, the steps are as follows:

1. A sequence of data stored in the document is input into Gowin Complex Multiplier IP.
2. The output is calculated by Complex Multiplier IP and compared to the correct data.

Design Example Application

This design example allows for quick verification of the functions of the Complex Multiplier. When using this reference design for board-level testing, users need to provide appropriate input stimulus. Signal observation can be performed using an on-chip logic analyzer or an oscilloscope.

