



Gowin CORDIC

Release Note

RN522-2.0E, 09/25/2020

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Revision History

Date	Version	Description
08/30/2018	1.0E	Initial version published.
03/28/2019	1.1E	Supported products updated.
09/25/2020	2.0E	Overview updated.

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1 About This Guide

This release includes the Gowin CORDIC IP reference design and user guide.

Gowin CORDIC IP user guide and reference design are available at [Gowin Website](#). The reference design has been configured with a case specific parameter, which can be used for simulation, instantiating the total integrated, total layout wiring after inserting the user design.

2 Overview

This time Gowin CORDIC IP extends the IP functions and optimizes the user guide. Detailed descriptions of the IP feature updated are as follows. Please refer to the user guide for details.

- Data bit width can be adjusted.
- Number of iterations can be adjusted.

Table 2-1 Gowin CORDIC IP Overview

Gowin CORDIC IP	
IP Core Application	
Supported Devices	GW all series
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	Gowin Software

3 Documents

The software release file contains Gowin CORDIC IP user guide, which is listed below:

Table 3-1 Gowin CORDIC IP Documents

Documents	Usage
Gowin CORDIC IP User Guide.pdf	PDF
Gowin CORDIC IP Release Note.pdf	PDF

4 IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and users can determine the location and timing constraints on his own.

For the customized IP design and support, please contact Gowin sales and support line.

Website: www.gowinsemi.com/en

E-mail: support@gowinsemi.com

