



Gowin AHB Bus Arbiter IP

Release Note

RN907-1.2E, 08/18/2023

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Revision History

Date	Version	Description
01/08/2020	1.0E	Initial version published.
07/19/2021	1.1E	● Gowin_EMPU_M1 software and hardware reference designs updated. ● Synplify Pro removed. ● Reference design updated.
08/18/2023	1.2E	Arora V FPGA products supported.

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1 About This Release

The released content of Gowin AHB Bus Arbiter IP includes:

- Arora V FPGA products supported

Gowin AHB Bus Arbiter IP reference design is available at Gowin Website. Take specific parameters as an example for the reference design, and the reference design can be used for simulation and overall synthesis, placement & routing after the instantiation with user design.

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Function and Enhancement Summary

The following table summarizes the functions and enhancements:

Function	Description
Front-end synthesis tool: GowinSynthesis V1.9.9 Beta-3	
Function	Arora V FPGA products supported
Back-end PnR tool: Gowin Software Gowin V1.9.9 Beta-3	
Enhancements	–
Device supported	All Devices

3 Platform Supported

The IP is supported on the platforms listed below:

Windows	Windows 7/8/10/11 (64 bits) Windows XP (32 bits)
Linux	Centos 6.8/7.0/7.5 (64 bits) Ubuntu 18.04/20.04 LTS

4 Documents

This IP release folder contains the documents listed below:

Documents	Description
IPUG907, Gowin AHB Bus Arbiter IP User Guide	PDF
RN907, Gowin AHB Bus Arbiter IP Release Note	PDF

5 IP Support

Since the requirements of user design and the maximum frequency are different, the reference design does not include FPGA specific location (.cst) and timing constraints (.sdc) documents, and you can determine the location and timing constraints on your own.

For the customized IP design and support, please contact Gowin sales.

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