



Gowin AHB Bus Arbiter IP

User Guide

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Revision History

Date	Version	Description
01/16/2020	1.0E	Initial version published.
07/19/2021	1.1E	● Gowin_EMPU_M1 software and hardware reference designs updated. ● Synplify Pro removed.
08/18/2023	1.2E	Arora V FPGA products supported.
12/31/2024	1.3E	● The IP category updated from Bus Bridge to Bus Interconnect. ● IP functions updated. ● The software programming reference design and hardware reference design updated.

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1 About This Guide

1.1 Purpose

The purpose of Gowin AHB Bus Arbiter IP User Guide is to help you to quickly understand the features and usage of Gowin AHB Bus Arbiter IP by providing descriptions of the functions, signal definition, working principle, and GUI, etc.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series SecureFPGA Products Data Sheet](#)
- [DS891, GW1NRF series Bluetooth FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Product Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
MCU	Microcontroller Unit
AHB	Advanced High performance Bus
GMD	Gowin MCU Designer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

Gowin AHB Bus Arbiter includes 16 Master device interfaces and one Slave device interface. Master device can be the MCU (Such as Gowin_EMPU_M1) or the FPGA logic modules with AHB bus protocol interfaces. Slave device can be the FPGA logic modules in accordance with the AHB bus protocol. The base address is 0x80000000.

Gowin AHB Bus Arbiter supports 32-bit standard AHB bus bit width and enhanced 64-bit AHB bus bit width, offering high speed and high bandwidth data communication.

The 16 Master device interfaces of Gowin AHB Bus Arbiter offer fixed priority arbitration. The priority is from high to low in turn from the first Master device interface to the 16th Master device interface.

2.2 Features

Gowin AHB Bus Arbiter features are as follows:

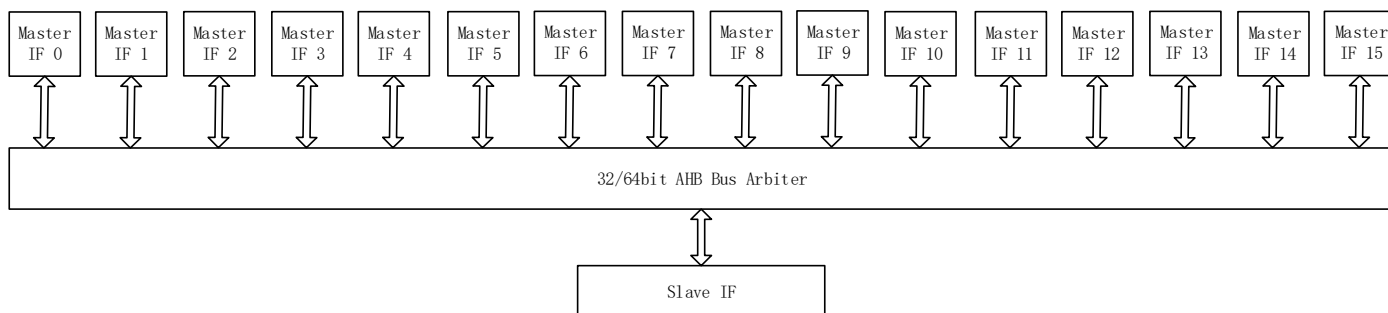
- Offers 16 Master device interfaces and one Slave device interface.
- Master device can be the MCU or the FPGA logic modules with AHB bus protocol interfaces.
- Supports 32-bit standard AHB bus bit width and enhanced 64-bit AHB bus bit width.
- Supports priority arbitration of the 16 Master device interfaces; the priority is from high to low in turn.

3 Working Principle

3.1 AHB Bus Arbitrator Model

As shown in Figure 3-1, AHB bus arbitrator model offers 16 Master device interfaces and one Slave device interface. The 16 Master devices can be the MCU or the FPGA logic modules with AHB bus protocol interfaces. The 16 Master device interfaces offers fixed priority. The priority is from high to low in turn from Master device interface 0 to Master device interface 15. Slave base address is 0x80000000. If the Master device is Gowin_EMPU_M1, it applies to AHB Master [1] bus extension interface.

Figure 3-1 AHB Bus Arbitrator Model



3.2 AHB Bus Arbitrator Mechanism

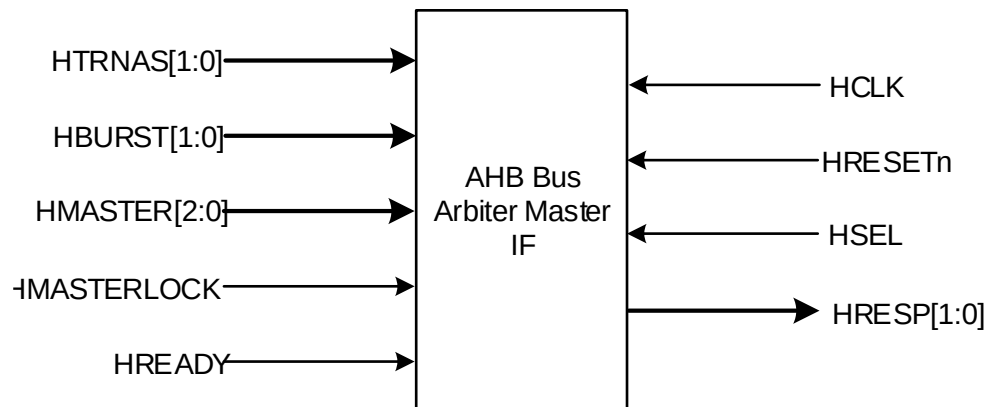
Arbitrator is the main manager of AHB system bus, used to monitor bus requests sent from Master devices, arbitrate the priority according to the internally set arbitration algorithm, and give the corresponding control signal. The bus adopts fixed priority algorithm. Only one Master device can occupy the bus at each moment. First requester will be responded first. If simultaneous requests, they will be responded according to priority. Each interaction is not allowed to be interrupted.

As shown in Figure 3-2, HCLK is clock signal, and HRESETn is reset signal.

- HSEL: Master device selects Slave device.

- HREADY: Slave device is ready.
- HTRANS: Bus interaction type, including IDLE, BUSY, NONSEQ, and SEQ.
- HRESP: Respond signal of interaction process, including OKAY, ERROR, RETRY, and SPLIT.
- HBURST: Burst type. Eight different burst interactions can be divided into SINGLE interaction, Variable length burst interaction (INCR), and fixed length burst interaction.
- HMASTER: Allows Master device to use Bus to decode. Only when this signal is valid, Master device can use Bus to decode.
- HMASTERLOCK: If it is valid, the interaction refers to the interaction of the locking sequence.

Figure 3-2 AHB Bus Arbitrator Mechanism



4 Signal Definition

The signal definition of Gowin AHB Bus Arbiter is as described in Table 4-1.

Table 4-1 Signal Definition of Gowin AHB Bus Arbiter

No.	Signal Name	I/O	Description	Remarks
1	HCLK	input	System clock signal	-
2	HRESETn	input	System reset signal	-
3	SHRDATAM0	input	Slave read data bus	Slave Slave IF (Default configuration)
4	SHREADYOUTM0	input	Slave HREADY feedback to master	
5	SHRESPM0	input	Slave transfer response	
6	SHSELM0	output	Slave select	
7	SHADDRM0	output	Slave address bus	
8	SHTRANSM0	output	Slave transfer type	
9	SHWRITEM0	output	Slave transfer direction	
10	SHSIZEM0	output	Slave transfer size	
11	SHBURSTM0	output	Slave burst type	
12	SHPROTM0	output	Slave protection control	
13	SHMASTERM0	output	Slave master select	
14	SHWDATAM0	output	Slave write data bus	
15	SHMASTLOCKM0	output	Slave locked sequence	
16	SHREADYMUXM0	output	Slave transfer done	
17	MHSELS0	input	Master IF_0 slave select	Arbiter Master IF 0
18	MHADDRS0	input	Master IF_0 address bus	
19	MHTRANSS0	input	Master IF_0 transfer type	
20	MHWITES0	input	Master IF_0 transfer direction	
21	MHSIZES0	input	Master IF_0 transfer size	
22	MHBURSTS0	input	Master IF_0 burst type	

No.	Signal Name	I/O	Description	Remarks
23	MHPROTS0	input	Master IF_0 protection control	
24	MHMASTERS0	input	Master IF_0 master select	
25	MHWDATAS0	input	Master IF_0 write data bus	
26	MHMASTLOCKS0	input	Master IF_0 locked sequence	
27	MHREADYS0	input	Master IF_0 transfer done	
28	MHRDATAS0	output	Master IF_0 read data bus	
29	MHREADYOUTS0	output	Master IF_0 HREADY feedback from slave	
30	MHRESPS0	output	Master IF_0 transfer response	Arbiter Master IF 1
31	MHSELS1	input	Master IF_1 slave select	
32	MHADDRS1	input	Master IF_1 address bus	
33	MHTRANSS1	input	Master IF_1 transfer type	
34	MHWITES1	input	Master IF_1 transfer direction	
35	MHSIZES1	input	Master IF_1 transfer size	
36	MHBURSTS1	input	Master IF_1 burst type	
37	MHPROTS1	input	Master IF_1 protection control	
38	MHMASTERS1	input	Master IF_1 master select	
39	MHWDATAS1	input	Master IF_1 write data bus	
40	MHMASTLOCKS1	input	Master IF_1 locked sequence	
41	MHREADYS1	input	Master IF_1 transfer done	
42	MHRDATAS1	output	Master IF_1 read data bus	
43	MHREADYOUTS1	output	Master IF_1 HREADY feedback from slave	
44	MHRESPS1	output	Master IF_1 transfer response	
45	MHSELS2	input	Master IF_2 slave select	Arbiter Master IF 2
46	MHADDRS2	input	Master IF_2 address bus	
47	MHTRANSS2	input	Master IF_2 transfer type	
48	MHWITES2	input	Master IF_2 transfer direction	
49	MHSIZES2	input	Master IF_2 transfer size	
50	MHBURSTS2	input	Master IF_2 burst type	
51	MHPROTS2	input	Master IF_2 protection control	
52	MHMASTERS2	input	Master IF_2 master select	
53	MHWDATAS2	input	Master IF_2 write data bus	
54	MHMASTLOCKS2	input	Master IF_2 locked sequence	
55	MHREADYS2	input	Master IF_2 transfer done	
56	MHRDATAS2	output	Master IF_2 read data bus	
57	MHREADYOUTS2	output	Master IF_2 HREADY feedback from slave	
58	MHRESPS2	output	Master IF_2 transfer response	Arbiter Master IF 3
59	MHSELS3	input	Master IF_3 slave select	

No.	Signal Name	I/O	Description	Remarks
60	MHADDRS3	input	Master IF_3 address bus	
61	MHTRANS3	input	Master IF_0 transfer type	
62	MHWRTS3	input	Master IF_3 transfer direction	
63	MHSIZES3	input	Master IF_3 transfer size	
64	MHBURSTS3	input	Master IF_3 burst type	
65	MHPROTS3	input	Master IF_3 protection control	
66	MHMASTERS3	input	Master IF_3 master select	
67	MHWDATAS3	input	Master IF_3 write data bus	
68	MHMASTLOCKS3	input	Master IF_3 locked sequence	
69	MHREADY3	input	Master IF_3 transfer done	
70	MHRDATAS3	output	Master IF_3 read data bus	
71	MHREADYOUTS3	output	Master IF_3 HREADY feedback from slave	
72	MHRESPS3	output	Master IF_3 transfer response	Arbiter Master IF 4
73	MHSELS4	input	Master IF_4 slave select	
74	MHADDRS4	input	Master IF_4 address bus	
75	MHTRANS4	input	Master IF_4 transfer type	
76	MHWRTS4	input	Master IF_4 transfer direction	
77	MHSIZES4	input	Master IF_4 transfer size	
78	MHBURSTS4	input	Master IF_4 burst type	
79	MHPROTS4	input	Master IF_4 protection control	
80	MHMASTERS4	input	Master IF_4 master select	
81	MHWDATAS4	input	Master IF_4 write data bus	
82	MHMASTLOCKS4	input	Master IF_4 locked sequence	
83	MHREADY4	input	Master IF_4 transfer done	
84	MHRDATAS4	output	Master IF_4 read data bus	
85	MHREADYOUTS4	output	Master IF_4 HREADY feedback from slave	
86	MHRESPS4	output	Master IF_4 transfer response	
87	MHSELS5	input	Master IF_5 slave select	Arbiter Master IF 5
88	MHADDRS5	input	Master IF_5 address bus	
89	MHTRANS5	input	Master IF_5 transfer type	
90	MHWRTS5	input	Master IF_5 transfer direction	
91	MHSIZES5	input	Master IF_5 transfer size	
92	MHBURSTS5	input	Master IF_5 burst type	
93	MHPROTS5	input	Master IF_5 protection control	
94	MHMASTERS5	input	Master IF_5 master select	
95	MHWDATAS5	input	Master IF_5 write data bus	
96	MHMASTLOCKS5	input	Master IF_5 locked sequence	
97	MHREADY5	input	Master IF_5 transfer done	

No.	Signal Name	I/O	Description	Remarks
98	MHRDATAS5	output	Master IF_5 read data bus	
99	MHREADYOUTS5	output	Master IF_5 HREADY feedback from slave	
100	MHRESPS5	output	Master IF_5 transfer response	
101	MHSELS6	input	Master IF_6 slave select	Arbiter Master IF 6
102	MHADDRS6	input	Master IF_6 address bus	
103	MHTRANS6	input	Master IF_6 transfer type	
104	MHWWRITES6	input	Master IF_6 transfer direction	
105	MHSIZES6	input	Master IF_6 transfer size	
106	MHBURSTS6	input	Master IF_6 burst type	
107	MHPROTS6	input	Master IF_6 protection control	
108	MHMASTERS6	input	Master IF_6 master select	
109	MHWWRITES6	input	Master IF_6 write data bus	
110	MHMASTLOCKS6	input	Master IF_6 locked sequence	
111	MHREADY6	input	Master IF_6 transfer done	
112	MHRDATAS6	output	Master IF_6 read data bus	
113	MHREADYOUTS6	output	Master IF_6 HREADY feedback from slave	
114	MHRESPS6	output	Master IF_6 transfer response	
115	MHSELS7	input	Master IF_7 slave select	Arbiter Master IF 7
116	MHADDRS7	input	Master IF_7 address bus	
117	MHTRANS7	input	Master IF_7 transfer type	
118	MHWWRITES7	input	Master IF_7 transfer direction	
119	MHSIZES7	input	Master IF_7 transfer size	
120	MHBURSTS7	input	Master IF_7 burst type	
121	MHPROTS7	input	Master IF_7 protection control	
122	MHMASTERS7	input	Master IF_7 master select	
123	MHWWRITES7	input	Master IF_7 write data bus	
124	MHMASTLOCKS7	input	Master IF_7 locked sequence	
125	MHREADY7	input	Master IF_7 transfer done	
126	MHRDATAS7	output	Master IF_7 read data bus	
127	MHREADYOUTS7	output	Master IF_7 HREADY feedback from slave	
128	MHRESPS7	output	Master IF_7 transfer response	
129	MHSELS8	input	Master IF_8 slave select	Arbiter Master IF 8
130	MHADDRS8	input	Master IF_8 address bus	
131	MHTRANS8	input	Master IF_8 transfer type	
132	MHWWRITES8	input	Master IF_8 transfer direction	
133	MHSIZES8	input	Master IF_8 transfer size	
134	MHBURSTS8	input	Master IF_8 burst type	

No.	Signal Name	I/O	Description	Remarks
135	MHPROTS8	input	Master IF_8 protection control	
136	MHMASTERS8	input	Master IF_8 master select	
137	MHWDATAS8	input	Master IF_8 write data bus	
138	MHMASTLOCKS8	input	Master IF_8 locked sequence	
139	MHREADYS8	input	Master IF_8 transfer done	
140	MHRDATAS8	output	Master IF_8 read data bus	
141	MHREADYOUTS8	output	Master IF_8 HREADY feedback from slave	
142	MHRESPS8	output	Master IF_8 transfer response	
143	MHSELS9	input	Master IF_9 slave select	Arbiter Master IF 9
144	MHADDRS9	input	Master IF_9 address bus	
145	MHTRANS9	input	Master IF_9 transfer type	
146	MHWWRITES9	input	Master IF_9 transfer direction	
147	MHSIZES9	input	Master IF_9 transfer size	
148	MHBURSTS9	input	Master IF_9 burst type	
149	MHPROTS9	input	Master IF_9 protection control	
150	MHMASTERS9	input	Master IF_9 master select	
151	MHWDATAS9	input	Master IF_9 write data bus	
152	MHMASTLOCKS9	input	Master IF_9 locked sequence	
153	MHREADYS9	input	Master IF_9 transfer done	
154	MHRDATAS9	output	Master IF_9 read data bus	
155	MHREADYOUTS9	output	Master IF_9 HREADY feedback from slave	
156	MHRESPS9	output	Master IF_9 transfer response	
157	MHSELS10	input	Master IF_10 slave select	Arbiter Master IF 10
158	MHADDRS10	input	Master IF_10 address bus	
159	MHTRANS10	input	Master IF_10 transfer type	
160	MHWWRITES10	input	Master IF_10 transfer direction	
161	MHSIZES10	input	Master IF_10 transfer size	
162	MHBURSTS10	input	Master IF_10 burst type	
163	MHPROTS10	input	Master IF_10 protection control	
164	MHMASTERS10	input	Master IF_10 master select	
165	MHWDATAS10	input	Master IF_10 write data bus	
166	MHMASTLOCKS10	input	Master IF_10 locked sequence	
167	MHREADYS10	input	Master IF_10 transfer done	
168	MHRDATAS10	output	Master IF_10 read data bus	
169	MHREADYOUTS10	output	Master IF_10 HREADY feedback from slave	
170	MHRESPS10	output	Master IF_10 transfer response	
171	MHSELS11	input	Master IF_11 slave select	Arbiter Master IF 11

No.	Signal Name	I/O	Description	Remarks
172	MHADDRS11	input	Master IF_11 address bus	
173	MHTRANSS11	input	Master IF_0 transfer type	
174	MHWITES11	input	Master IF_11 transfer direction	
175	MHSIZES11	input	Master IF_11 transfer size	
176	MHBURSTS11	input	Master IF_11 burst type	
177	MHPROTS11	input	Master IF_11 protection control	
178	MHMASTERS11	input	Master IF_11 master select	
179	MHWDATAS11	input	Master IF_11 write data bus	
180	MHMASTLOCKS11	input	Master IF_11 locked sequence	
181	MHREADYS11	input	Master IF_11 transfer done	
182	MHRDATAS11	output	Master IF_11 read data bus	
183	MHREADYOUTS11	output	Master IF_11 HREADY feedback from slave	
184	MHRESPS11	output	Master IF_11 transfer response	
185	MHSELS12	input	Master IF_12 slave select	Arbiter Master IF 12
186	MHADDRS12	input	Master IF_12 address bus	
187	MHTRANSS12	input	Master IF_0 transfer type	
188	MHWITES12	input	Master IF_12 transfer direction	
189	MHSIZES12	input	Master IF_12 transfer size	
190	MHBURSTS12	input	Master IF_12 burst type	
191	MHPROTS12	input	Master IF_12 protection control	
192	MHMASTERS12	input	Master IF_12 master select	
193	MHWDATAS12	input	Master IF_12 write data bus	
194	MHMASTLOCKS12	input	Master IF_12 locked sequence	
195	MHREADYS12	input	Master IF_12 transfer done	
196	MHRDATAS12	output	Master IF_12 read data bus	
197	MHREADYOUTS12	output	Master IF_12 HREADY feedback from slave	
198	MHRESPS12	output	Master IF_12 transfer response	
199	MHSELS13	input	Master IF_13 slave select	Arbiter Master IF 13
200	MHADDRS13	input	Master IF_13 address bus	
201	MHTRANSS13	input	Master IF_13 transfer type	
202	MHWITES13	input	Master IF_13 transfer direction	
203	MHSIZES13	input	Master IF_13 transfer size	
204	MHBURSTS13	input	Master IF_13 burst type	
205	MHPROTS13	input	Master IF_13 protection control	
206	MHMASTERS13	input	Master IF_13 master select	
207	MHWDATAS13	input	Master IF_13 write data bus	
208	MHMASTLOCKS13	input	Master IF_13 locked sequence	
209	MHREADYS13	input	Master IF_13 transfer done	

No.	Signal Name	I/O	Description	Remarks
210	MHRDATAS13	output	Master IF_13 read data bus	
211	MHREADYOUTS13	output	Master IF_13 HREADY feedback from slave	
212	MHRESPS13	output	Master IF_13 transfer response	
213	MHSELS14	input	Master IF_14 slave select	Arbiter Master IF 14
214	MHADDRS14	input	Master IF_14 address bus	
215	MHTRANS14	input	Master IF_14 transfer type	
216	MHWWRITES14	input	Master IF_14 transfer direction	
217	MHSIZES14	input	Master IF_14 transfer size	
218	MHBURSTS14	input	Master IF_14 burst type	
219	MHPROTS14	input	Master IF_14 protection control	
220	MHMASTERS14	input	Master IF_14 master select	
221	MHWWRITES14	input	Master IF_14 write data bus	
222	MHMASTLOCKS14	input	Master IF_14 locked sequence	
223	MHREADY14	input	Master IF_14 transfer done	
224	MHRDATAS14	output	Master IF_14 read data bus	
225	MHREADYOUTS14	output	Master IF_14 HREADY feedback from slave	
226	MHRESPS14	output	Master IF_14 transfer response	
227	MHSELS15	input	Master IF_15 slave select	Arbiter Master IF 15
228	MHADDRS15	input	Master IF_15 address bus	
229	MHTRANS15	input	Master IF_15 transfer type	
230	MHWWRITES15	input	Master IF_15 transfer direction	
231	MHSIZES15	input	Master IF_15 transfer size	
232	MHBURSTS15	input	Master IF_15 burst type	
233	MHPROTS15	input	Master IF_15 protection control	
234	MHMASTERS15	input	Master IF_15 master select	
235	MHWWRITES15	input	Master IF_15 write data bus	
236	MHMASTLOCKS15	input	Master IF_15 locked sequence	
237	MHREADY15	input	Master IF_15 transfer done	
238	MHRDATAS15	output	Master IF_15 read data bus	
239	MHREADYOUTS15	output	Master IF_15 HREADY feedback from slave	
240	MHRESPS15	output	Master IF_15 transfer response	

5 Parameter Definition

The parameter definition of Gowin AHB Bus Arbiter is as described in Table 5-1.

Table 5-1 Parameter Definition of Gowin AHB Bus Arbiter

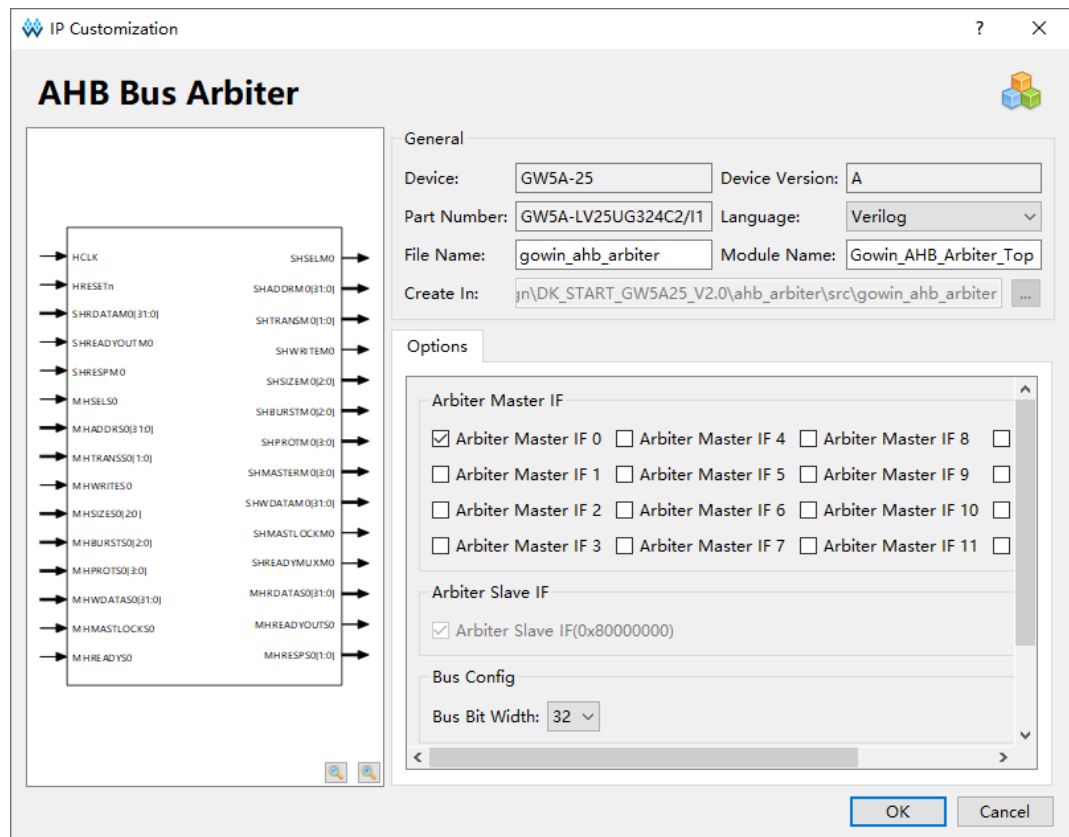
No.	Name	Description	Value
1	Arbiter Master IF 0	Configure the first Arbiter Master interface	Enable/Disable
2	Arbiter Master IF 1	Configure the second Arbiter Master interface	Enable/Disable
3	Arbiter Master IF 2	Configure the third Arbiter Master interface	Enable/Disable
4	Arbiter Master IF 3	Configure the fourth Arbiter Master interface	Enable/Disable
5	Arbiter Master IF 4	Configure the fifth Arbiter Master interface	Enable/Disable
6	Arbiter Master IF 5	Configure the sixth Arbiter Master interface	Enable/Disable
7	Arbiter Master IF 6	Configure the seventh Arbiter Master interface	Enable/Disable
8	Arbiter Master IF 7	Configure the eighth Arbiter Master interface	Enable/Disable
9	Arbiter Master IF 8	Configure the ninth Arbiter Master interface	Enable/Disable
10	Arbiter Master IF 9	Configure the tenth Arbiter Master interface	Enable/Disable
11	Arbiter Master IF 10	Configure the eleventh Arbiter Master interface	Enable/Disable
12	Arbiter Master IF 11	Configure the twelfth Arbiter Master interface	Enable/Disable
13	Arbiter Master IF 12	Configure the thirteenth Arbiter Master interface	Enable/Disable
14	Arbiter Master IF 13	Configure the fourteenth Arbiter Master interface	Enable/Disable
15	Arbiter Master IF 14	Configure the fifteenth Arbiter Master interface	Enable/Disable
16	Arbiter Master IF 15	Configure the sixteenth Arbiter Master interface	Enable/Disable
17	Arbiter Slave IF	Configure Arbiter Slave interface	Enable
18	Bus Bit Width	Configure AHB bus width	32/64

6 GUI Configuration

You can use IP core generator tool in the IDE to call and configure Gowin AHB Bus Arbiter IP. Select "Tools > IP Core Generator" on the menu bar or click "  " on the tool bar to open the IP Core Generator, and select "Soft IP Core > Microprocessor System > Bus Interconnect > AHB Bus Arbiter 1.2".

Gowin AHB Bus Arbiter configuration interface is as shown in Figure 6-1.

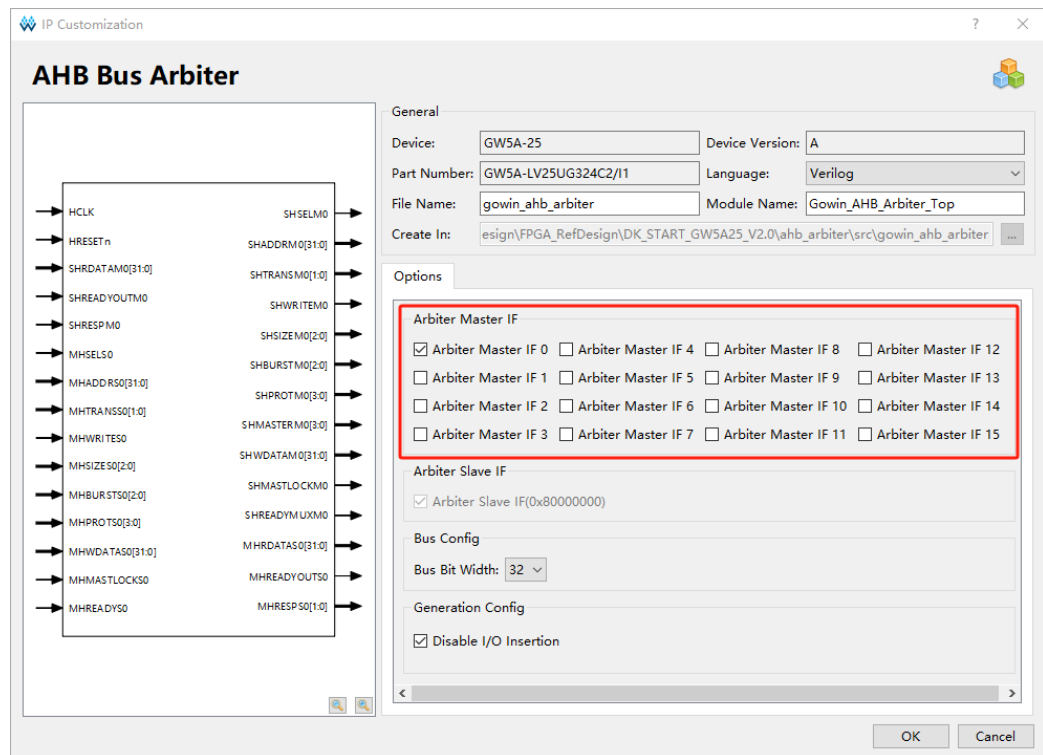
Figure 6-1 Gowin AHB Bus Arbiter Configuration Interface



6.1 Arbiter Master IF Configuration

Arbiter Master IF Configuration is as shown in Figure 6-2.

Figure 6-2 Aribter Master IF Configuration



- If "Arbiter Master IF 0" is selected, the first Master interface will be configured and output;
- If "Arbiter Master IF 1" is selected, the second Master interface will be configured and output;
- If "Arbiter Master IF 2" is selected, the third Master interface will be configured and output;
- If "Arbiter Master IF 3" is selected, the fourth Master interface will be configured and output;
- If "Arbiter Master IF 4" is selected, the fifth Master interface will be configured and output;
- If "Arbiter Master IF 5" is selected, the sixth Master interface will be configured and output;
- If "Arbiter Master IF 6" is selected, the seventh Master interface will be configured and output;
- If "Arbiter Master IF 7" is selected, the eighth Master interface will be configured and output;
- If "Arbiter Master IF 8" is selected, the ninth Master interface will be configured and output;
- If "Arbiter Master IF 9" is selected, the tenth Master interface will be

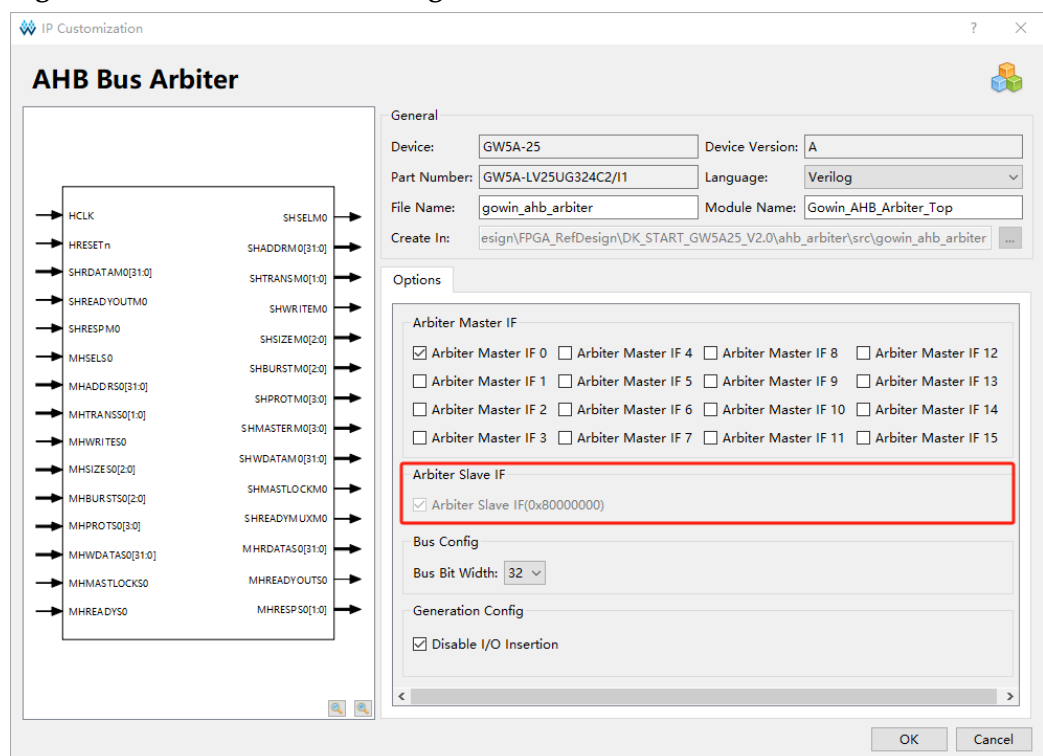
configured and output;

- If "Arbiter Master IF 10" is selected, the eleventh Master interface will be configured and output;
- If "Arbiter Master IF 11" is selected, the twelfth Master interface will be configured and output;
- If "Arbiter Master IF 12" is selected, the thirteenth Master interface will be configured and output;
- If "Arbiter Master IF 13" is selected, the fourteenth Master interface will be configured and output;
- If "Arbiter Master IF 14" is selected, the fifteenth Master interface will be configured and output;
- If "Arbiter Master IF 15" is selected, the sixteenth Master interface will be configured and output;

6.2 Arbiter Slave IF Configuration

AHB Bus Arbiter supports one Slave device. The default configuration is Arbiter Slave IF (0x80000000), as shown in Figure 6-3.

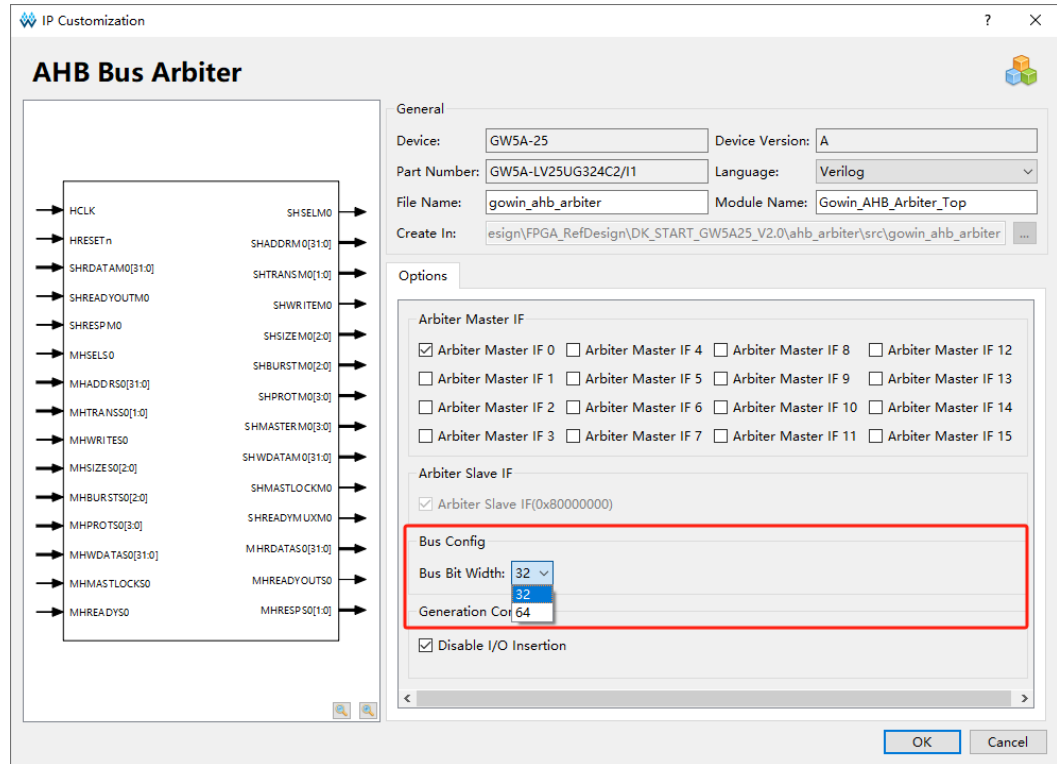
Figure 6-3 Arbiter Slave IF Configuration



6.3 Bus Bit Width Configuration

AHB Bus Arbiter bus bit width configuration is as shown in Figure 6-4.

Figure 6-4 Bus Bit Width Configuration



- If 32 bits is selected, the AHB Bus Arbiter bit width is standard 32-bit;
- If 64 bits is selected, the AHB Bus Arbiter bit width is enhanced 64-bit;
- The AHB Bus Arbiter bit width is 32-bit by default.

7 Reference Design

Please refer to Gowin AHB Bus Arbiter [Reference Design](#) for details at Gowinsemi website:

- Hardware reference
design: ...\\ref_design\FPGA_RefDesign\DK_START_GW5A25_V2.0\\ahb_arbiter
- Software programming reference
design: ...\\ref_design\MCU_RefDesign\\ahb_arbiter

