



Gowin Integer Multiply Divider IP

Release Note

RN539-1.0E,1/30/2019

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Revision History

Date	Version	Description
1/30/2019	1.0E	Initial version published.

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About This Guide

Gowin Integer Multiply Divider IP user guide is released.

Gowin Integer Multiply Divider IP user guide is available at Gowin website: www.gowinsemi.com. Specific parameters had been taken as an example for the reference design, which can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

Overview

Gowin Integer Multiply Divider IP completes signed and unsigned Integer multiplication, division calculation, including radix mode, which can be adjusted as needed.

Table 1 Gowin DIVIDER IP Overview

Gowin Integer Multiply Divider	
IP Core Application	
Supported Devices	GW1N series GW1NR series GW1NS series GW1NZ series GW2A series GW2AR series
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GoWinYunYuan

Document

The software release file contains Gowin Integer Multiply Divider IP User Guide, which is listed below:

Figure 2 Gowin Integer Multiply Divider IP Document

Document	Usage
Gowin Integer Multiply Divider User Guide	PDF
Gowin Integer Multiply Divider Release Note	PDF

IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not include associated FPGA specific location (.cst) and timing constraints (.sdc) documents, which the user can determine by himself as required.

For the customized IP design and support, please contact Gowin sales and support line.

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