



Gowin Integer Multiply Divider IP

User Guide

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Revision History

Date	Version	Description
02/22/2019	1.0E	Initial version published.
10/24/2019	1.1E	● Supported devices updated; ● Timing description updated; ● The description of calculation mode added.
09/09/2020	1.2E	● Table 2-2 and Table 2-3 added; ● Resource utilization updated.

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1 About This Guide

1.1 Purpose

The purpose of Gowin Integer Multiply Divider IP User Guide is to help users learn the features and usage of Gowin Integer Multiply Divider IP by providing the description of the functions, ports, timing, GUI and reference design.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. [DS100](#), GW1N series of FPGA Products Data Sheet
2. [DS117](#), GW1NR series of FPGA Products Data Sheet
3. [DS821](#), GW1NR series FPGA Products Data Sheet
4. [DS871](#), GW2AR series of FPGA Products Data Sheet
5. [DS881](#), GW2AR series of FPGA Products Data Sheet
6. [DS861](#), GW1NR series FPGA Products Data Sheet
7. [DS102](#), GW2A series of FPGA Products Data Sheet
8. [DS226](#), GW2AR series of FPGA Products Data Sheet
9. [SUG100](#), Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
Register	Register

Terminology and Abbreviations	Meaning
ALU	Arithmetic Logical Unit
LUT	Look-up Table

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

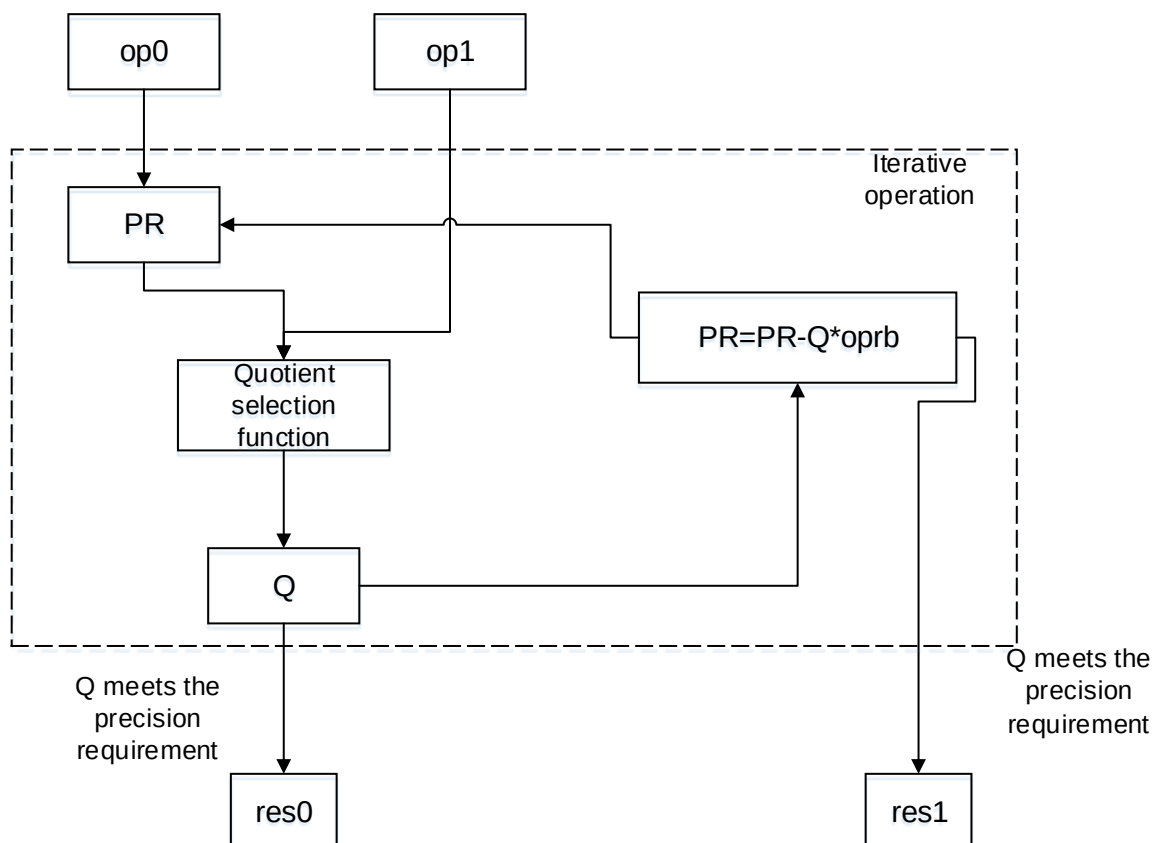
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin Integer Multiply Divider IP can realize signed and unsigned integer multiplication and division operations. The diagram is shown as Figure 2-1.

Figure 2-1 Integer Multiply Divider Block Diagram



2.1 Introduction to Integer Multiply Divider IP

Gowin Integer Multiply Divider IP is designed to realize integer multiplication and division operations with less logic resources.

Table 2-1 Gowin Integer Multiply Divider IP Overview

Gowin Integer Multiply Divider IP	
Supported Devices	GW1N Series: GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, GW1N-9; GW1NR Series, GW1NS Series, GW1NSE Series, GW1NSE Series, GW1NSR Series, GW2A Series, GW2AR Series.
Logic Resource	See Table 2-4.
Delivered Doc.	
Design Files	Verilog
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify Pro
Application Software	Gowin Software

2.2 Features and Performance

2.2.1 Features

- Supports signed and unsigned integer division operation;
- Supports signed and unsigned Integer multiplication operation;
- The latency is related to the parameters configuration;
- Can be configured to radix2, 4, 16, and fast modes;
- Port dynamic selection is supported;
- Supports urgent suspension;
- Supports calculation history tags.

2.2.2 Max. Frequency

The max. frequency of Gowin Integer Multiply Divider IP is mainly determined by speed grade of the selected devices.

2.2.3 Latency

The latency is mainly determined by the input data and the calculation mode.

Table 2-2 Multiplication Latency

Function	Radix	Latency	Remarks
Multiplication	fast	5/6	The positive multiplies the positive is 5, and there is a negative in the operation is 6.
	radix2	33/34	The positive multiplies the positive is 33, and there is a negative in the operation is 34.
	radix4	17/18	The positive multiplies the positive is 17, and there is a negative in the operation is 18.
	radix16	9/10	The positive multiplies the positive is 9, and there is a negative in the operation is 10.

Table 2-3 Division Latency

Function	Input data	Latency	Remarks
Division	N/N	$(DN1 \geq DN2) ?$ $(4 + DN1 - DN2) : 4$	● DP: The lowest bit of which left bits are 0; ● DN: The lowest bit of which left bits are 1; ● DP1, DN1: Dividend; ● DP2, DN2: Divisor.
	P/N	$(DP1 \geq DN2) ?$ $(4 + DP1 - DN2) : 4$	
	N/P	$(DN1 \geq DP2) ?$ $(4 + DN1 - DP2) : 4$	
	P/P	$(DP1 \geq DP2) ?$ $(3 + DP1 - DP2) : 3$	

Note !

P represents a positive number and N represents a negative number.

2.2.4 Resource Utilization

Integer Multiply Divider can be realized by Verilog language. Its performance and resource utilization may vary when the design is employed in different devices, or at different densities, speeds, or grades.

Take the GW2A-55 device as an example. Gowin Integer Multiply Divider IP resource utilization is shown in Table 2-4. For the applications in the other GOWINSEMI devices, please refer to the later release.

Table 2-4 Resource Utilization

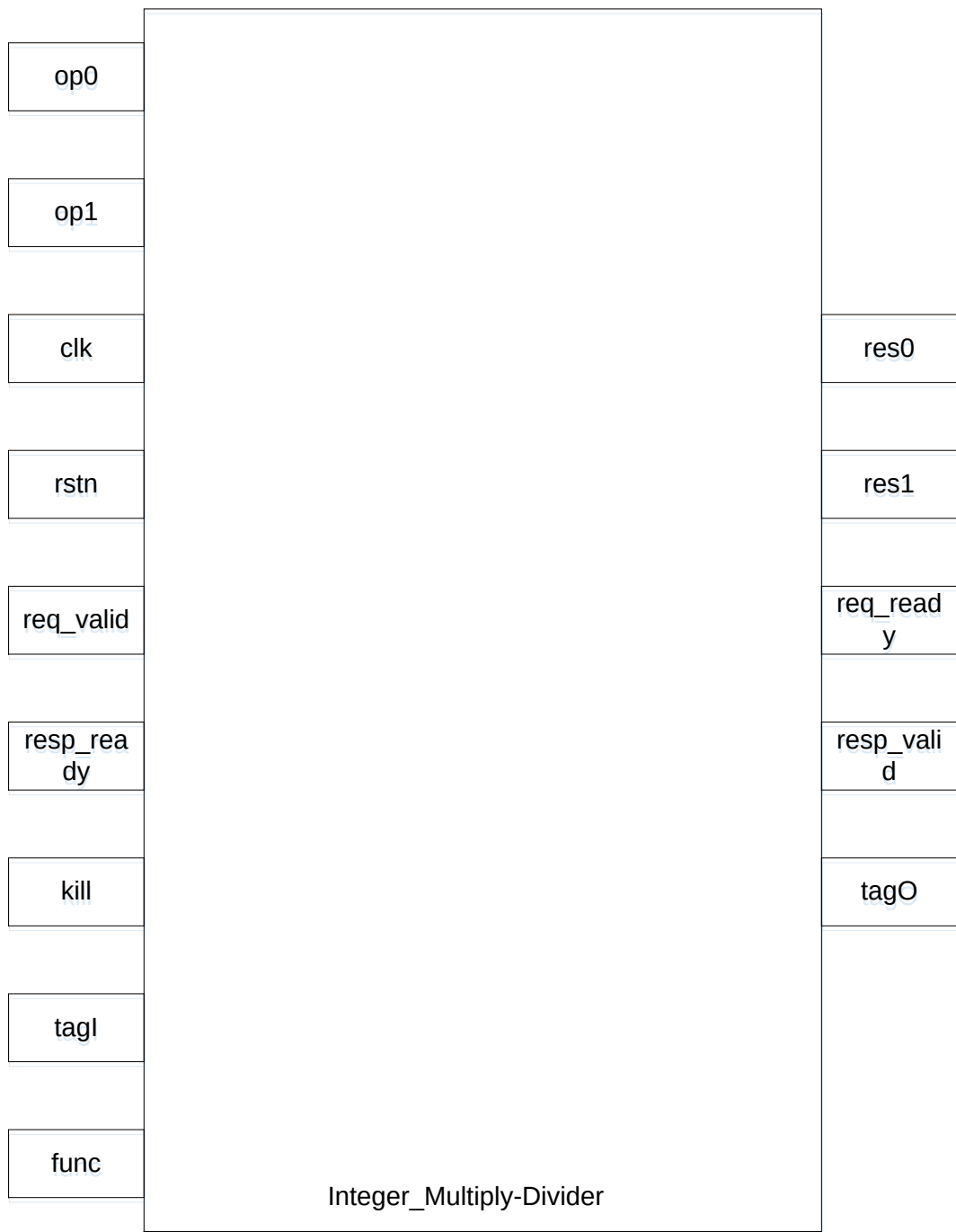
Device	Speed Grade	Resource Name	Resource Utilization
GW2A-55	C8/I7	CFU Logics	1525(1317LUTs,208 ALUs)
		CLSs (used)	848
		Registers	187

3 Functional Description

3.1 Structure and Function

Gowin Integer Multiply Divider IP can realize signed and unsigned integer multiplication and division operations. And you can configure parameters as required when generating the module. The diagram is as shown in Figure 3-1.

Figure 3-1 Integer Multiply Divider Interface Diagram



You input data op0 and op1 and determine multiplication or division operation through func signal. IP will generate results (multiplication operation can output res0 or res1 as results, and division operation can output res0 and res1 as quotient and remainder).

3.2 Calculation Mode

Table 3-1 Calculation Mode

Mode Selection	Function	op0	op1	res0	res1
4'b0000(MUL)	Signed Multiplication	Multiplier (32-bit signed)	Multiplier (32-bit signed)	Product lower 32 bits	Product upper 32 bits
4'b0001(MULH)	Signed Multiplication	Multiplier (32-bit signed)	Multiplier (32-bit signed)	Product upper 32 bits	Product upper 32 bits
4'b0010(MULHU)	Unsigned Multiplication	Multiplier (32-bit unsigned)	Multiplier (32-bit unsigned)	Product upper 32 bits	Product upper 32 bits
4'b0011(MULHSU)	Signed*Unsigned	Multiplier (32-bit signed)	Multiplier (32-bit unsigned)	Product upper 32 bits	Product upper 32 bits
4'b0100(DIV)	Signed/Unsigned	Dividend (32-bit signed)	Divisor (32-bit signed)	Quotient	Remainder
4'b0101(DIVU)	Signed/Unsigned	Dividend (32-bit unsigned)	Divisor (32-bit unsigned)	Quotient	Remainder
4'b0110(REM)	Signed*Unsigned Multiplication	Dividend (32-bit signed)	Divisor (32-bit signed)	Remainder	Remainder
4'b0111(remu)	Signed*Unsigned Multiplication	Dividend (32-bit unsigned)	Divisor (32-bit unsigned)	Remainder	Remainder

Note!

- The signed here are two's complement.
- When the user ports are insufficient, it can choose to connect res0 port. At this time, if the division operation is performed, the quotient can be obtained through DIV mode, and then the remainder can be obtained through REM mode.

3.3 Configure Radix

You can configure to radix2, 4, 16, and fast modes. The radix multiplier option implements the multiplier by serial addition, while the fast multiplier option implements a two-stage pipelining parallel multiplier. The calculation speed is fast > radix16 > radix4 > radix2.

3.4 Data Bit Width

Currently it supports up to 32 bits width.

4 Port Description

The details of Gowin Integer Multiply Divider IP I/O ports are shown in Table 4-1, and the diagram is as shown in Figure 3-1.

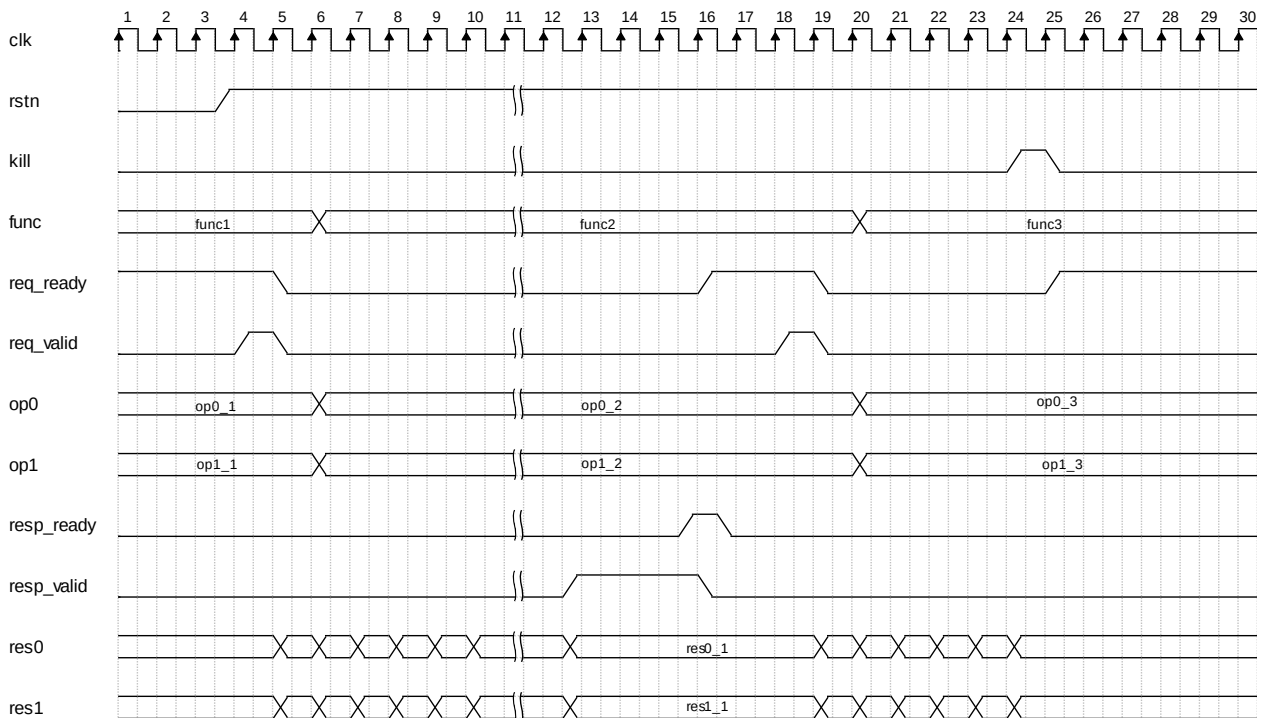
Table 4-1 I/O Port List

Signal	I/O	Description
op0	Input	Operand 0
op1	Input	Operand 1
res0	Output	Result 0
res1	Output	Result 1
clk	Input	Clock signal
rstn	Input	Reset signal, active - low
req_valid	Input	Request valid signal
req_ready	Output	Request ready signal
resp_valid	Output	Response valid signal
resp_ready	Input	Response ready signal
kill	Input	Kill process signal
tagI	Input	Input tag signal
tagO	Output	Output tag signal
func	Input	Function selected signal

5 Timing Description

This section introduces the timing of Gowin Integer Multiply Divider IP as shown in Figure 5-1.

Figure 5-1 Signal Timing



As shown in Figure 5-1, you can input data when *req_ready* is high. In the non-reset state (*rstn*=1), when the clock *clk* samples the first *req_valid* signal at high level, Gowin Integer Multiply Divider IP will use the input data *op0*, *op1* and the calculation mode corresponding to the *func* signal to calculate and pull down the *req_ready* signal. After that, the *req_valid* signal will be invalid until the *req_ready* is pulled up again. During the calculation, *res0* and *res1* are output for each clock cycle, but this result is inaccurate and is not recommended. When the *resp_valid* is high, it indicates that the *res0* and *res1* are already valid i.e. *res0_1* and *res1_1* in

the above figure. It should be noted that a complete calculation period is not completed at this time. You need to pull up the `resp_ready` signal to indicate that the calculated data have been received. At this time, the Integer Multiply Divider IP will pull down `resp_valid` signal to indicate that the output is invalid at this time and the `req_ready` signal will be pulled up to indicate that the new input data and `func` signal can be received. So far, a complete calculation is completed. The calculation time from input to output depends on the radix mode.

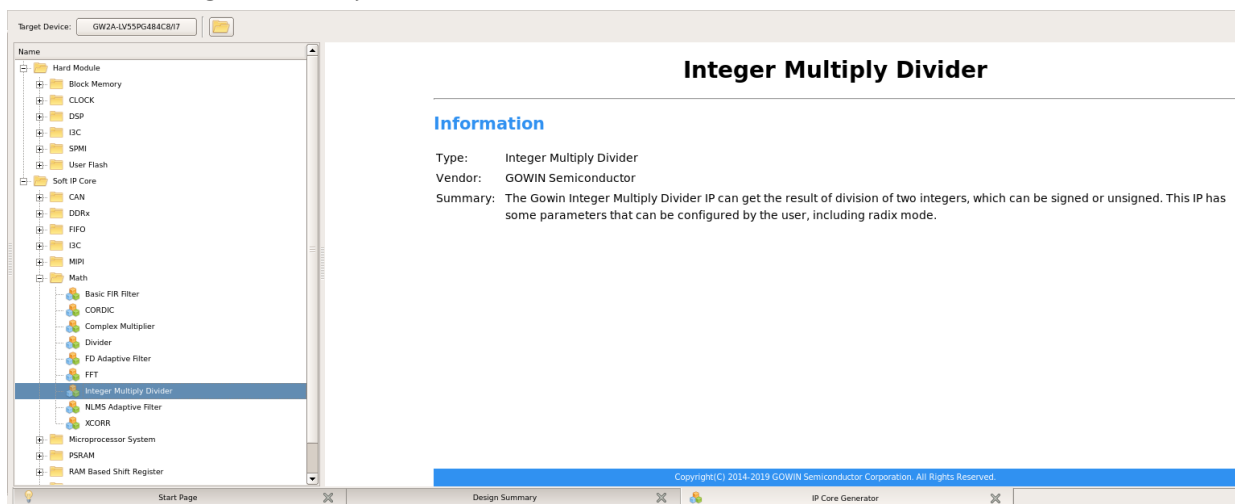
If the calculation needs to be stopped urgently, you can pull up `kill` signal, and the IP will be pull up `req_ready`, indicating that the data and `func` signal can be received again.

6 GUI

Start "IP Core Generator" from the "Tools" menu in the Gowin software, then invoke and configure Integer Multiply Divider IP.

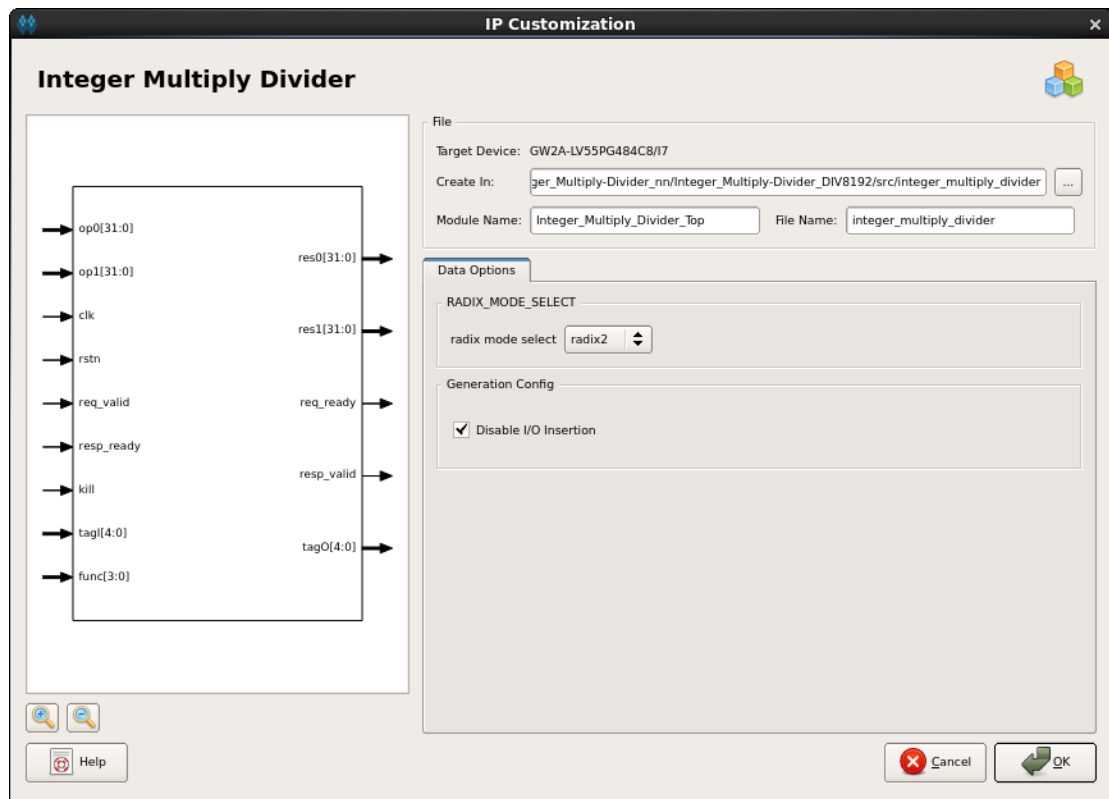
1. Create a project, as shown in Figure 6-1.

Figure 6-1 Project View



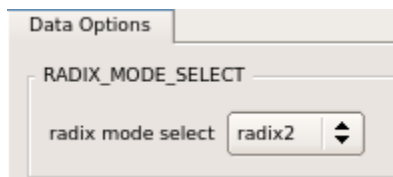
2. Open Integer Multiply Divider IP
Click "IP Core Generator > Soft IP Core > Integer Multiply Divider" to open Integer Multiply Divider IP view, as shown in Figure 6-2.

Figure 6-2 Integer Multiply Divider IP View



3. As shown in Figure 6-3, you can configure the radix mode. You can generate the Integer Multiply Divider IP by clicking "OK" after configuring the parameters as required.

Figure 6-3 Parameters View



7 Reference Design

See the [ref_design](#) for details.

8 Documents Delivered

It includes two parts: document and reference design. The document folder contains user guide.

Table 8-1 Document List

Name	Description
IPUG539, Gowin Integer Multiply Divider IP User Guide	Gowin Integer Multiply Divider IP User Guide

