



Gowin PCI to Ethernet IP

User Guide

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1 About This Guide

1.1 Purpose

The purpose of Gowin PCI to Ethernet IP is to help you learn the features and usage of Gowin PCI to Ethernet IP by providing the description of features, ports, configuration and call.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com/en:

- [DS100](#), GW1N series of FPGA Products Data Sheet
- [DS102](#), GW2A series of FPGA Products Data Sheet
- [DS117](#), GW1NR series of FPGA Products Data Sheet
- [DS226](#), GW2AR series of FPGA Products Data Sheet
- [DS821](#), GW1NS series of FPGA Products Data Sheet
- [DS841](#), GW1NZ series of FPGA Products Data Sheet
- [DS861](#), GW1NSR series of FPGA Products Data Sheet
- [DS871](#), GW1NSE series of SecureFPGA Products Data Sheet
- [DS881](#), GW1NSER series of SecureFPGA Products Data Sheet
- [DS891](#), GW1NRF series of Bluetooth FPGA Products Data Sheet
- [DS961](#), GW2ANR series of FPGA Products Data Sheet
- [DS971](#), GW2AN series of FPGA Products Data Sheet
- [SUG100](#), Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Meaning

Terminology and Abbreviations	Meaning
IP	Intellectual Property
LUT	Look-up Table

Terminology and Abbreviations	Meaning
PCI	Peripheral Component Interconnect
Ethernet	Ethernet

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com/en

E-mail: support@gowinsemi.com

2 Overview

Gowin PCI to Ethernet IP allows you to configure Gowin Triple Speed Ethernet IP through PCI bus, realizing communication between Gowin PCI Target IP and Gowin Triple Speed Ethernet IP.

Table 2-1 Gowin PCI to Ethernet IP Overview

Gowin PCI to Ethernet IP	
Supported Devices	All devices (excluding 1K resource devices such as GW1N-1/GW1N-1S/GW1NZ-1)
Logic Resource	See Table 2-2
Delivered Doc.	
Design Files	Verilog (encryption)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

2.1 Primary Function

The primary function of Gowin PCI to Ethernet IP is to enable a PCI device to communicate with an Ethernet device, which is mounted on a base of the PCI as a back-end device.

2.2 Working Frequency

The Gowin PCI Target IP operates at 33 MHz and the Gowin Triple Speed Ethernet Controller IP operates at 125 MHz, so the two IP working clock are asynchronous clocks. And the PCI to Ethernet IP processes across clock domains.

2.3 Resource Utilization

Gowin PCI to Ethernet IP is designed in Verilog and Table 2-2 gives an overview of resources utilization based on GW2A55 devices. For application verification on other Gowin FPGAs, please pay attention to the post-released information.

Table 2-2 Resources Utilization

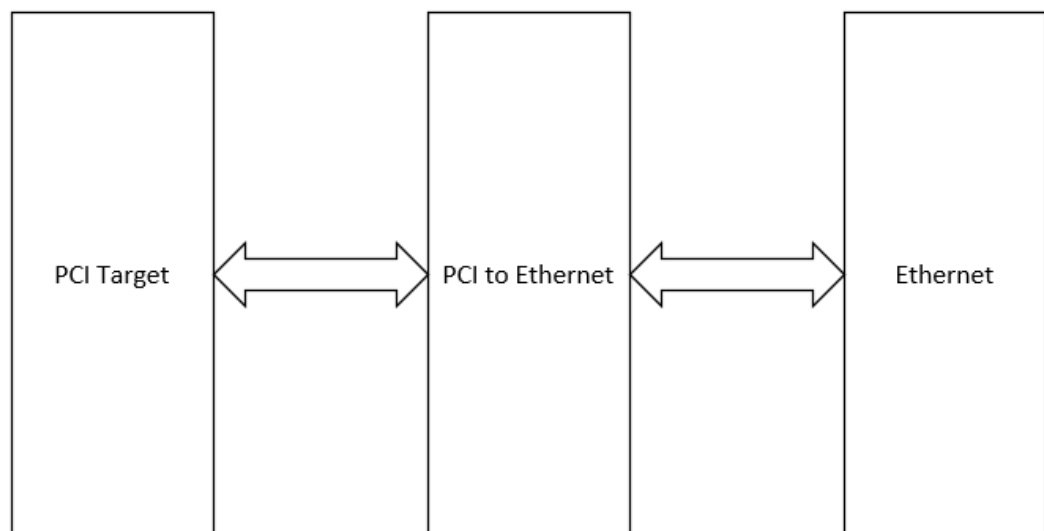
LUTs	REGs	Block Rams	Device Series	Speed Level
921	668	4	GW2A-55	-8

3 Functional Description

3.1 System Block Diagram

As shown in Figure 3-1, PCI to Ethernet is between the Local end interface of PCI Target and the front-end interface of Ethernet, which realizes interface conversion from PCI to Ethernet and communication.

Figure 3-1 PCI to Ethernet Block Diagram



3.2 Functional Block Diagram Description

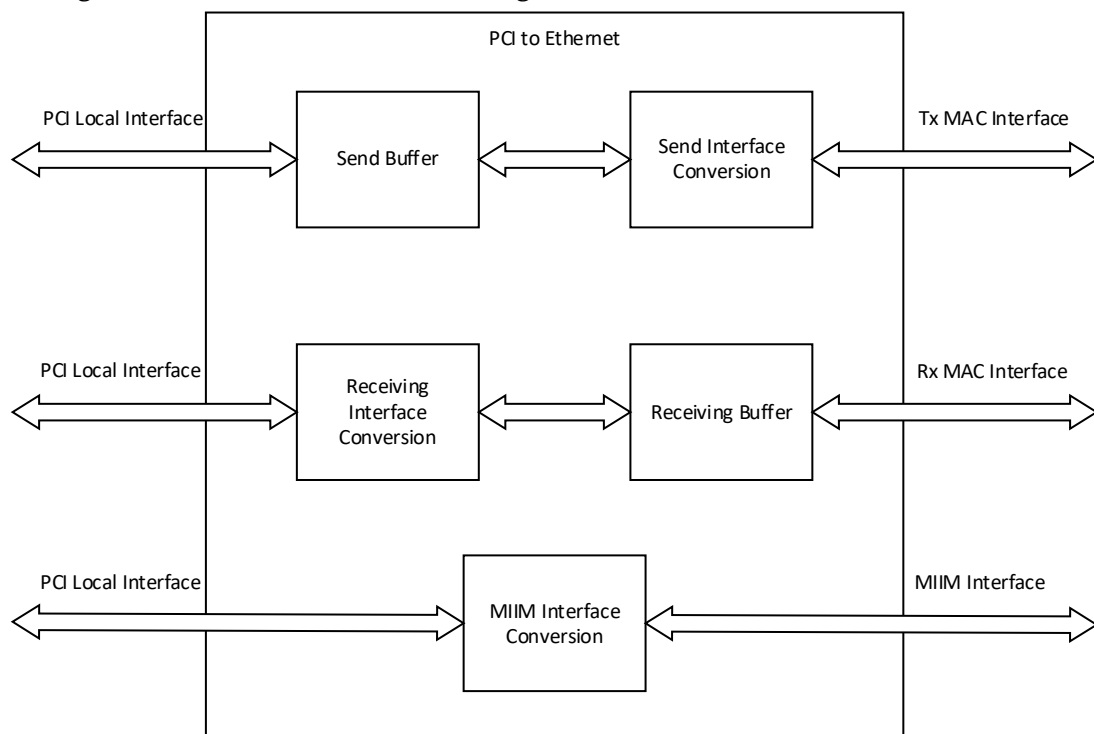
Gowin PCI to Ethernet IP consists of five modules, as shown in Figure 3-2.

- The function of the Send Buffer Module is to cache the data sent by PCI. The Send Buffer can contain the maximum length of an Ethernet frame, i.e., an Ethernet frame of 1518 bytes.
- The function of the Send Interface Conversion Module is to convert the PCI data format to the data format required by the Tx MAC interface of Ethernet IP and to generate the control signals for the associated Tx MAC interface.
- The function of the Receiving Buffer module is to cache the data sent

by Ethernet. The receiving Buffer can contain the maximum length of an Ethernet frame, i.e., an Ethernet frame of 1518 bytes.

- The function of the Receiving Interface Conversion Module is to convert the data format of Rx MAC interface of Ethernet IP to the data format required by the PCI and to generate the control signals for the associated Local interface.
- The function of MIIM interface conversion module is to convert between the PCI Local interface and the Ethernet IP MIIM interface to each other without the need for caching due to the small amount of data.

Figure 3-2 PCI to Ethernet Block Diagram



3.3 Register Information

Table 3-1 shows the register group of PCI to Ethernet. Since the maximum address of the register is 0x1014, the base address register of the PCI Target IP should be set to at least 128KB. A description of each register address mapping is shown in the table below.

Table 3-1 Register Information

Offset/Range	Name	Access Restriction	Functional Description
0x0000-0x0fff	MIIM Configure	None	MIIM Configuration Register When this register is accessed, a portion of the address of tg_addr is mapped to the phyad and regad of the Ethernet MIIM interface as follows: 11:7 => phyad (0x0 by default)

Offset/Range	Name	Access Restriction	Functional Description
			6:2 => regad (0x0 by default) When a read and write data request is initiated to this segment address, the data mapping is as follows: In the case of write transfer, the data sent by PCI is mapped to miim_wrdata[15:0] in the MIIM interface; in the case of read transfer, PCI reads the data from miim_rddata[15:0] in the MIIM interface.
0x1000	Speed Configure	WO	Ethernet Rate and Duplex Configuration Registers The Ethernet operating rate (10M/100M/1000M) and duplex mode (half-duplex or full-duplex) can be configured by writing data. 0 => speedis1000 (0x0 by default) 1 => speedis10 (0x0 by default) The above two [1:0] are available in the following combinations. 00=> 100M 01=> 1000M 10=> 10M 2 => duplex_status A bit of 0 indicates full duplex, and a bit of 1 indicates half duplex.
0x1004	Tx Frame Length	None	Send Frame Length Register Prior to PCI sending data to Ethernet, the total number of bytes of Ethernet frames to be sent is written to this register. Then Ethernet data can be sent to the Send Buffer Register.
0x1008	Tx State	Read-only	Send State Register You can know how the Ethernet data is sent by reading the data in this register. A read data of 0

Offset/Range	Name	Access Restriction	Functional Description
			indicates that the Ethernet data has not been sent. A read data of 1 indicates that the Ethernet data has been sent.
0x100c	Tx Data	Write-only	Send Data Register When PCI sends data to this register, the data goes into the Send Buffer Module, and when a frame of data has been sent, the Tx MAC interface timing is generated to complete the data transfer.
0x1010	Rx Frame Length	Read-only	Receive Frame Length Register PCI needs to read the value in this register before it can receive Ethernet data. This register stores the number of bytes of Ethernet frames in the Receive Buffer. And it can determine the number of read operations PCI needs to perform based on the read data.
0x1014	Rx Data	Read-only	Receive Data Register When PCI accesses this register as read, it can read the Ethernet data in the receive buffer.

3.4 Operating Flow

You need to determine which base of PCI mounts Ethernet. Note that the tg_bar_hit signal of PCI Target can be 1 to 6 bits width, and the tg_bar_hit signal of PCI to Ethernet is 1 bit width. Therefore, one of the bits of tg_bar_hit needs to be connected to the tg_bar_hit, which can satisfy the operation of PCI Target on different bases.

The operating flow of Gowin PCI to Ethernet IP is described below.

1. Configure Speed Configure to determine the working rate and duplex mode of the Ethernet.
2. Configure MIIM Configure to determine the properties and working modes of the PHY chip.
3. Send receiving data
 - If you want to send data, write an Ethernet frame length (in bytes) to the Tx Frame Length register, then you can send data to Tx

Data.

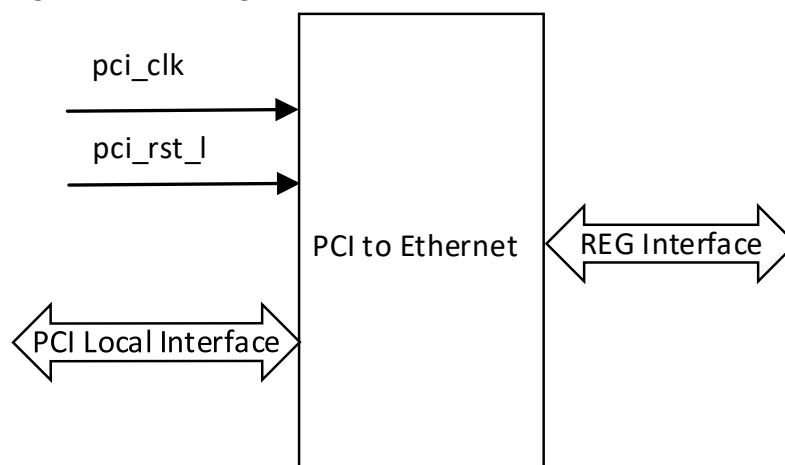
- If you want to receive data, read an Ethernet frame length (in bytes) to the Rx Frame Length register, then you can send data Rx Data.

For details on Gowin PCI Target IP and Gowin Triple Speed Ethernet IP, please refer to [IPUG904](#), Gowin PCI Target IP User Guide and [IPUG538](#), Gowin Triple Speed Ethernet IP User Guide.

4 Interface Description

4.1 Pin Diagram

Figure 4-1 Pin Diagram of PCI to Ethernet



4.2 Pin Description

Table 4-1 Pin Description

Pin	I/O	Description	Notes
Clock and Reset			All signals take PCI to Ethernet IP as reference.
pci_clk	Input	PCI Input Clock	
pci_reset_l	Input	Asynchronous Reset Signal, active-low.	
gtx_clk	Input	125M Clock Input. When Ethernet TX uses RGMII or GMII interface, 125MHz clock should be input.	
PCI Local Interface			
tg_addr[31:0]	Input	PCI Target address signal	
tg_data_out[31:0]	Input	PCI Target data output signal during write operation.	
tg_data_in[31:0]	Output	PCI Target data input signal during read operation.	
tg_cbe_l[3:0]	Input	PCI Target byte enable signal, active-low.	
tg_ready_l	Output	When the signal is valid, it indicates that PCI to Ethernet is ready to receive or transmit data, active-low.	
tg_write_l	Input	PCI Target write operation indicator, active-low.	
tg_read_l	Input	PCI Target read operation indicator, active-low.	
tg_stop_l	Output	Transmission stop signal, active-low.	
tg_abort_l	Output	Transmission abort signal, active-low.	
tg_cmd_o[3:0]	Input	PCI Target transmission command signal	
tg_bar_hit	Input	Single-bit base selection signal. This signal comes from one bit of the tg_bar_hit[5:0] signals on the PCI Target, which can be customized and can mount Ethernet IP on the required base.	
tg_access	Input	When this signal is valid, it indicates that PCI Target is accessing the local	

Pin	I/O	Description	Notes
		interface.	
tg_value	Input	When the signal is valid, it indicates that the data on tg_data_out[31:0] and tg_data_in[31:0] is valid during write/read operations.	
Ethernet IP Interface			
speedis1000	Output	Select signal based on Ethernet rate. When Ethernet IP works in RGMII or GMII/MII mode, configure IP to work at 1000M rate or 10M/100M rate: 1:1000M 0:10M/100M	
speedis10	Output	Select signal based on Ethernet rate. When IP works in RGMII mode and speedis1000 is 0, the configured IP works at 10M or 100M rate: 1:10M 0:100M It is should be noted when speedis1000 is1, this configuration pin is ignored.	
duplex_status	Output	Ethernet duplex mode configures signal. When IP works in RGMII, MII or GMII/MII mode, configure IP working duplex mode : 1:half duplex 0:full duplex	
rx_mac_clk	Input	The user receives clock.	
rx_mac_valid	Input	The user receives enable.	
rx_mac_data	Input	The user receives data.	
rx_mac_last	Input	The user side receives the indication of last byte	
rx_mac_error	Input	The user side receives the indication of error frame.	
rx_pause_req	Input	Receiving the signal of pause frame.	
rx_pause_val	Input	Receiving pause frame parameter field represents the pause time required by the party.	

Pin	I/O	Description	Notes
rx_statistics_valid	Input	The user receives the indication of valid statistics.	
rx_statistics_vector	Input	The user receives statistics.	
tx_mac_clk	Output	The user transmits clock.	
tx_mac_valid	Output	The user transmits enable.	
tx_mac_data	Output	The user transmits data.	
tx_mac_last	Output	The user transmits the indication of last byte.	
tx_mac_error	Output	The user transmits the indication of error frame.	
tx_mac_ready	Output	The user transmits a handshake signal. It indicates that tx_mac_data is received with a value of 1.	
tx_collision	Input	The user side transmits the line collision indicator signal. When the value is 1, it indicates that there is a line collision in this transmission and the user needs to end this transmission immediately. This signal is valid only in half duplex.	
tx_retransmit	Input	The user side will transmit a retransmission indicator signal, which appears with tx_collision at the same time, and the value of 1 means that this frame needs to be retransmitted. This signal is valid only in half duplex.	
rx_fcs_fwd_ena	Output	Receiving FCS Forward function: 1: Enable receiving of the FCS Forward function. 0: Disable receiving of the FCS Forward function.	
rx_jumbo_ena	Output	Receiving Jumbo function: 1: Enable receiving Jumbo function. 0: Disable receiving Jumbo function.	
tx_pause_req	Output	Send enable signal of	

Pin	I/O	Description	Notes
		pause frame.	
tx_pause_val	Output	Send the parameter field of pause frame, which means the counterpart needs to pause time.	
tx_pause_source_addr	Output	Send the source address of pause frame.	
tx_ifg_delay_ena	Output	Transmitting the minimum IFG configuration enable: 1: Enable the minimum IFG configuration. 0: Disable the minimum IFG configuration, and the default minimum IFG is 12 bytes.	
tx_ifg_delay	Output	Transmitting minimum IFG: When tx_ifg_delay_ena is 1, the minimum IFG transmitted by IP is determined by tx_ifg_delay. When tx_ifg_delay is less than 8, the minimum IFG is 8. When tx_ifg_delay is greater than or equal to 8, the minimum IFG is set by the user. When tx_ifg_delay_ena is 0, this setting is invalid.	
tx_fcs_fwd_ena	Output	Transmitting FCS Forward Function 1: Enable send FCS Forward function. 0: Disable send FCS Forward function.	
tx_statistics_valid	Output	The user transmits the indication of valid statistics.	
tx_statistics_vector	Output	The user side transmits statistics.	
Clk	Input	Management module clock input	
miim_phyad	Output	PHY address	
miim_regad	Output	Address	
miim_wrdata	Output	Write data	
miim_wren	Output	Write enable	
miim_rden	Output	Read enable	

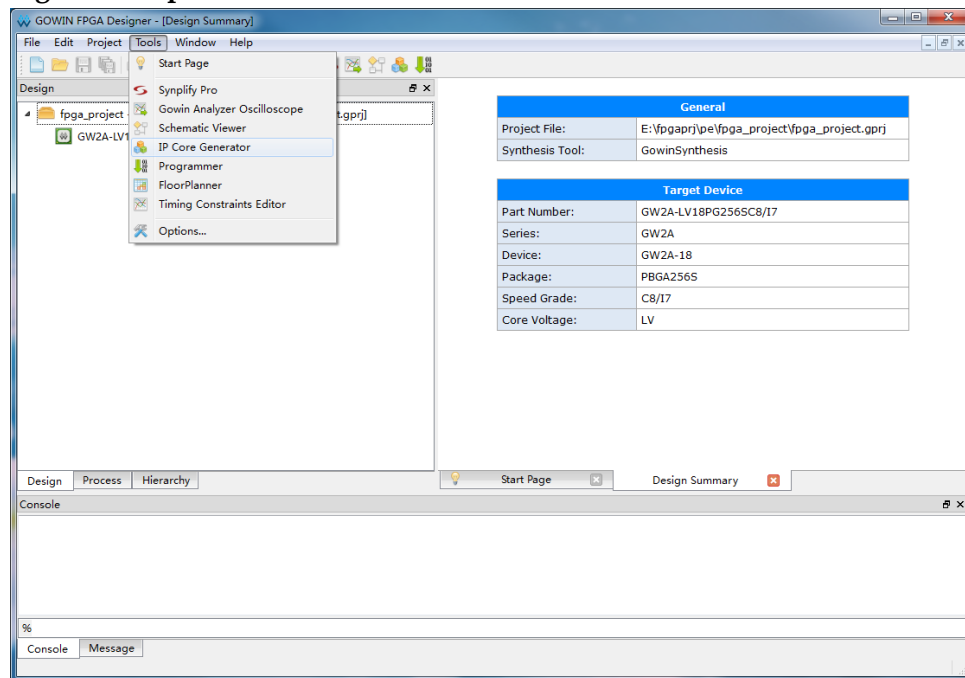
Pin	I/O	Description	Notes
miim_rddata	Input	Read data	
miim_rddata_valid	Input	Read data valid	
miim_busy	Input	MIIM interface status indicator: 1: Reading/Writing 0: Idle	

5 Interface Configuration

You can use IP core generator tool in the IDE to call and configure PCI to Ethernet IP.

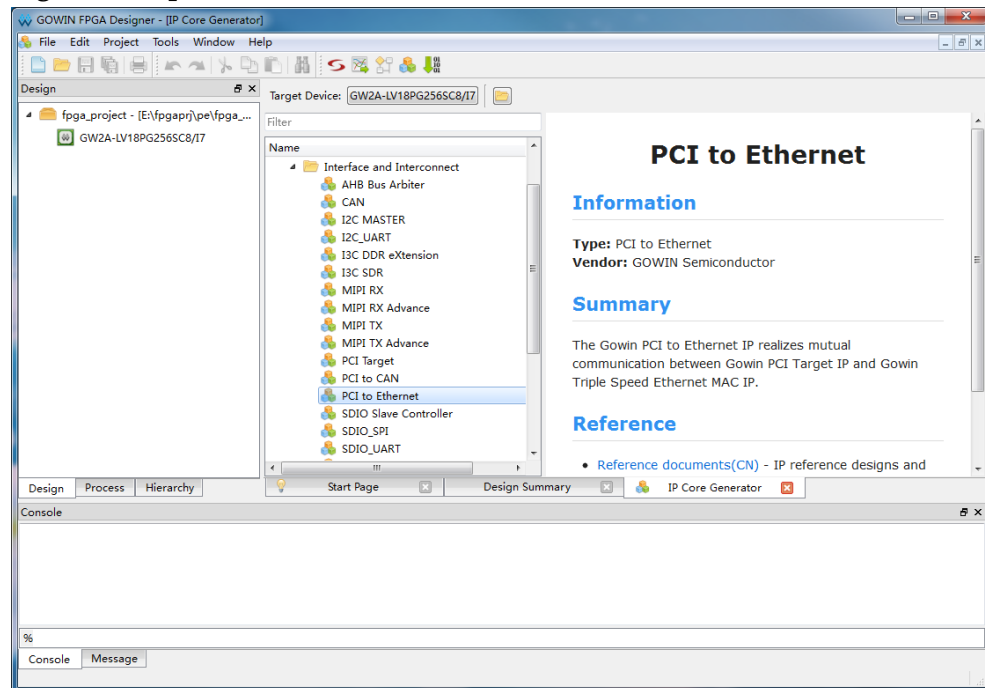
1. Open IP Core Generator. After creating the project, click the “Tools” tab, select and open the “IP Core Generator” from the drop-down list, as shown in Figure 5-1.

Figure 5-1 Open IP Core Generator



2. Open PCI to Ethernet IP Core
Click “Interface and Interconnect” and double click "PCI to Ethernet" to open the configuration interface, as shown in Figure 5-2.

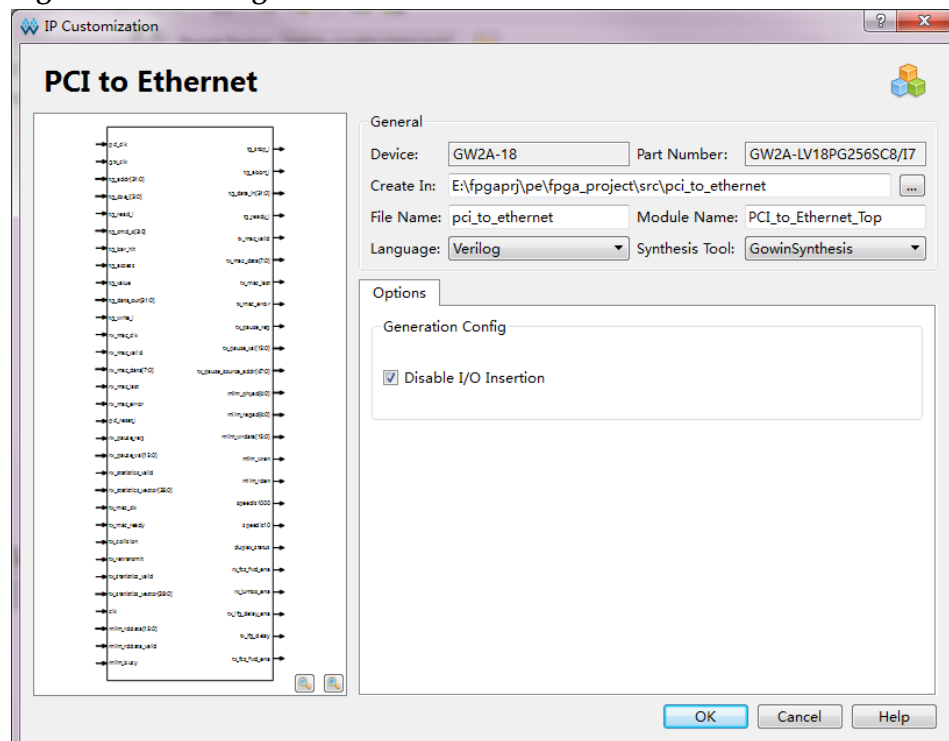
Figure 5-2 Open PCI to Ethernet IP Core



3. PCI to Ethernet IP Core Port Diagram

The left of the configuration interface is the port diagram of PCI to Ethernet IP Core, as shown in Figure 5-3.

Figure 5-3 Port Diagram of PCI to Ethernet IP



4. Open Help

Click "Help" button in the lower left corner in Figure 5-3 to learn the simple English introduction of configuration options, so as to help users

quickly complete the configuration of IP core. The order of options in Help is the same as the one in the interface, as shown in Figure 5-4.

Figure 5-4 Help

PCI to Ethernet

Information

Type: PCI to Ethernet
Vendor: GOWIN Semiconductor

Summary

The Gowin PCI to Ethernet IP realizes mutual communication between Gowin PCI Target IP and Gowin Triple Speed Ethernet MAC IP.

Reference

- [Reference documents\(CN\)](#) - IP reference designs and user guide
- [Reference documents\(EN\)](#) - IP reference designs and user guide

5. Configure the Basic Configuration Information

See the project basic information in the configuration interface. Take GW2A-18 chip as an example, and select the "PG256" package. The "Module Name" option displays the top-level file name of the generated project, and the default is "PCI_to_Ethernet_Top". You can modify the name. The folder generated by the IP core is shown in "File Name", which contains the files required by PCI to Ethernet IP core, and the default is "pci_to_ethernet". You can modify the path. "Create In" displays the path of IP core folder. The default is "\project path\src\pci_to_ethernet". You can modify the path.

Figure 5-5 Basic Information Configuration Interface

The screenshot shows a configuration window titled "General" with the following fields:

- Device:** GW2A-18
- Part Number:** GW2A-LV18PG256SC8/I7
- Create In:** E:\fpgapj\pe\fpga_project\src\pci_to_ethernet (with a browse button "...")
- File Name:** pci_to_ethernet
- Module Name:** PCI_to_Ethernet_Top
- Language:** Verilog (dropdown menu)
- Synthesis Tool:** GowinSynthesis (dropdown menu)

6 File Delivery

The delivery files for Gowin PCI to Ethernet IP includes documents and design source code.

6.1 Documents

The documents folder mainly contains the user guide in PDF.

Table 6-1 Documents List

Name	Description
IPUG754 , Gowin PCI to Ethernet IP User Guide	Gowin PCI to Ethernet User Guide

6.2 Design Source Code

The encrypted code file contains the RTL encrypted code of the Gowin PCI to Ethernet IP which is used for GUI in order to cooperate with Gowin software to generate the IP core required by users.

Table 6-2 Design Source Code List of PCI to Ethernet

Name	Description
pci_to_ethernet.v	The top-level file of the IP core, which provides users with interface information, encrypted.

