



Gowin PDM2PCM IP

User Guide

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Revision History

Date	Version	Description
12/06/2019	1.0E	Initial version published.
01/03/2020	1.1E	PLL removed.
09/30/2020	1.2E	Resources Structure Optimized.
01/05/2021	1.3E	Resources Structure Optimized.
04/28/2021	1.3.1E	The version information of Gowin Software added.
10/17/2025	1.4E	● Descriptions of 2.2 PDM2PCM Algorithm Introduction updated. ● Descriptions of 3.4 Resource Utilization updated. ● Section 1.2 Related Documents updated. ● The maximum frequency updated to 150 MHz. ● The timing diagrams updated. ● Configuration option descriptions added.
10/30/2025	1.4.1E	An example for generating CIC Compensation Filter coefficients added.

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1 About This Guide

1.1 Purpose

This Gowin PDM2PCM User Guide mainly includes the descriptions of the functions, features, ports, timing, call and configuration, and reference design, etc. It helps you quickly understand the features and usage of Gowin PDM2PCM IP.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com.

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CIC Filter	Cascaded Integrator Comb Filter
DSP	Digital Signal Processing
IP	Intellectual Property
LUT	Look-up Table
PCM	Pulse-code Modulation
PDM	Pulse-density Modulation
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

2.1 Gowin PDM2PCM IP

Gowin PDM2PCM IP is designed to convert PDM data to PCM data

Table 2-1 Gowin PDM2PCM IP Overview

Gowin PDM2PCM IP	
Logic Resource	Please refer to Table 3-1
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Gowin Synthesis
Application Software	Gowin Software (V1.9.7.03 and above)

Note!

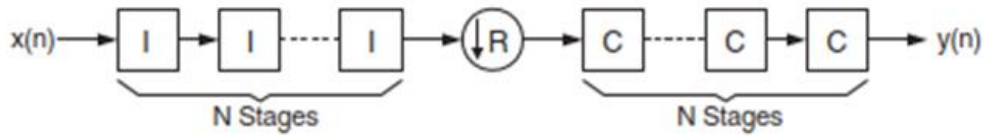
For the devices supported, you can click [here](#) to get the information.

2.2 PDM2PCM Algorithm Introduction

The implementation of PDM2PCM consists of two parts: a CIC Filter and a CIC Compensation Filter. Since PDM data is oversampled, the CIC Filter first downsamples it to twice the PCM sampling rate, and then the CIC Compensation Filter performs half-band filtering while providing inverse compensation for the CIC Filter.

CIC filter is an effective implementation of a moving average filter.

Figure 2-1 CIC Filter

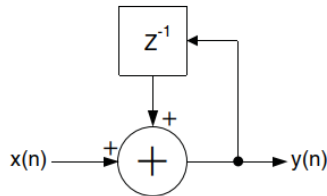


As shown in Figure 2-1, CIC Filter is a cascaded integrator comb filter. PDM2PCM uses the extraction structure of CIC filter and the input signal is processed successively by integrator, down sampling and comb filter.

The transfer function is

$$H(z) = H_I^N(z^R)H_C^N = \frac{(1 - Z^{-RM})^N}{(1 - Z^{-1})^N}$$

Figure 2-2 Integrator Filter



The integrator filter is as shown in Figure 2-2. The integrator is a one-pole IIR filter. The state equation is

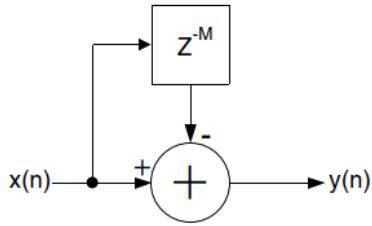
$$y[n] = y[n - 1] + x[n]$$

$y[n]$ is the current state output, $y[n - 1]$ is the last output, $x[n]$ is the current input.

The transfer function is

$$H_I(z) = \frac{1}{(1 - Z^{-1})}$$

Figure 2-3 Comb Filter



Comb filter is as shown in Figure 2-3. The comb filter is a symmetrical FIR filter. The state equation is

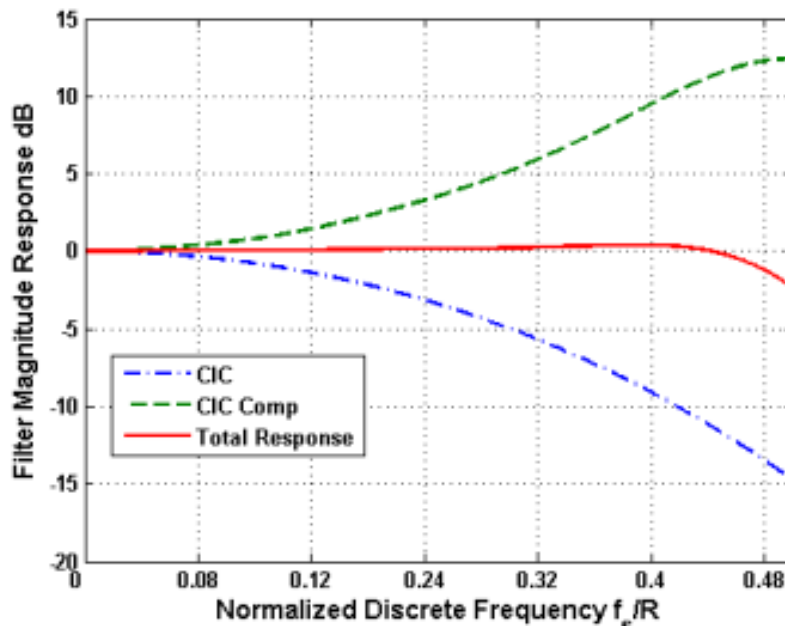
$$y[n] = x[n] - x[n - M]$$

$y[n]$ is the current state output, $x[n]$ is the current input, and $x[n - M]$ is the x input at $n-m$.

The transfer function is

$$H_C(z) = 1 - z^{-M}$$

Figure 2-4 CIC Compensation Filter



The issue with the CIC Filter is that its passband is not sufficiently flat and its stopband is not sufficiently attenuated. Although cascading multiple stages of CIC Filters can meet the requirements, a CIC Compensation Filter implemented using an FIR Filter is used to provide inverse compensation for the CIC Filter, ensuring a wider passband and adequate stopband attenuation.

3 Features and Performance

3.1 Features

- The number of PDM input channels can be configured (1-8 channels).
- Edge identification of PDM can be configured (posedge, negedge, double edges).
- Loading coefficients of the CIC Compensation Filter can be customized.

3.2 Max. Frequency

The maximum frequency of Gowin PDM2PCM IP is determined by the speed grade of the devices, and it can reach up to 150 MHz.

3.3 Latency

The latency of Gowin PDM2PCM IP is determined by the configuration parameters.

3.4 Resource Utilization

Gowin PDM2PCM IP can be implemented by Verilog. Its performance and resource utilization may vary when the design is employed in different devices, or at different density, speed, grade or the different modes of IP configuration.

Take Gowin GW2A-55 series of FPGA as an example to introduce the resource utilization of PDM2PCM. The resource utilization of PDM2PCM is shown in Table 3-1. For application verification on other Gowin FPGA, please pay attention to the later information.

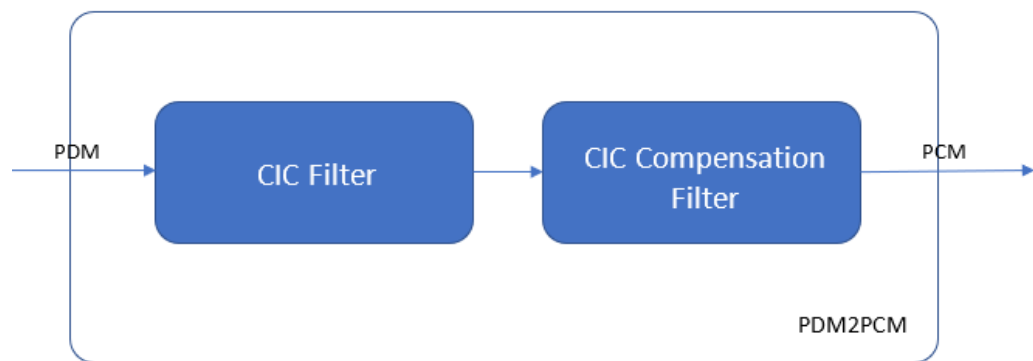
Table 3-1 Resource Utilization of Gowin PDM2PCM IP

Device Series	Speed Grade	Name	Resource Utilization	Remarks
GW2A-55	-8	LUT	2690	● Data bit width: 16 ● Number of channels: 8 ● Dual-edge detection ● Number of cascaded CIC Filters: 4 ● Number of CIC Compensation Filter taps: 64
		REG	5384	
		ALU	1586	
		BSRAM	4	
		SSRAM	34	
		DSP	2	

4 Functional Description

PDM2PCM is implemented through CIC Filter and CIC compensation Filter in FPGA and the block diagram is shown in Figure 4-1.

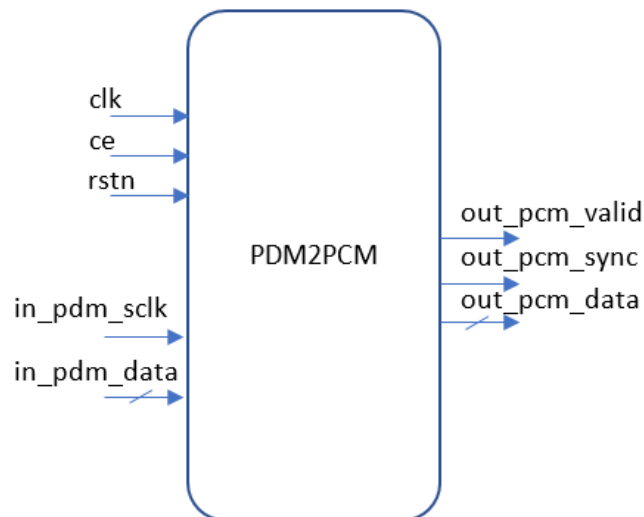
Figure 4-1 Block Diagram of PDM2PCM



5 Port Description

The IO ports of Gowin PDM2PCM IP are shown in Figure 5-1.

Figure 5-1 Ports of Gowin PDM2PCM IP



For Gowin PDM2PCM IP ports description details, please refer to Table 5-1.

Table 5-1 Gowin PDM2PCM IP IO List

Signal	I/O	Description
clk	Input	Clock input signal
ce	Input	Enable signal
rstn	Input	Reset signal, active-low
in_pdm_data	Input	PDM data input signal (The number of channel is the number of data bits)
in_pdm_sclk	input	PDM clock signal
out_pcm_valid	Output	PCM data output valid signal

Signal	I/O	Description
out_pcm_sync	Output	PCM data synchronization signal
out_pcm_data	Output	PCM data output signal

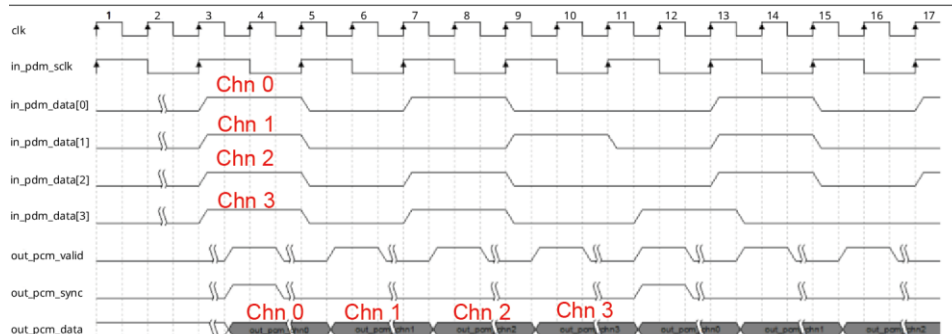
6 Timing Description

This chapter is intended to introduce the timing of Gowin PDM2PCM IP.

6.1 Single Edge Timing of PDM2PCM

The timing diagram of PDM2PCM (4-channel) Positive/Negative Edge Mode state is shown in Figure 6-1.

Figure 6-1 Timing Diagram of PDM2PCM (4-channel) Positive/Negative Edge Mode State



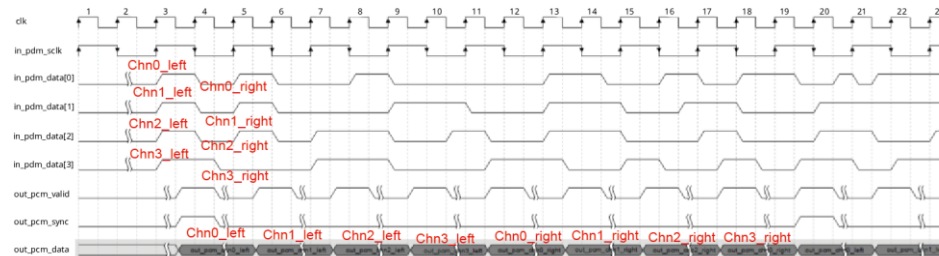
Gowin PDM2PCM IP outputs PDM clock signals (out_pdm_sclk) according to requirements of users.

The PDM input valid data (in_pdm_data[0-N]) of multiple channels is obtained for top/bottom edge sampling. And the IP outputs valid data for multiple channels after a period of time. Each channel is distinguished by a synchronous signal (out_pcm_sync).

6.2 Double Edge Timing of PDM2PCM

The timing diagram of PDM2PCM (4-channel) Double Edge Mode state is shown in Figure 6-2.

Figure 6-2 Timing Diagram of PDM2PCM (4-channel) Double Edge Mode State



Gowin PDM2PCM IP outputs PDM clock signals (out_pdm_sclk) according to requirements of users.

The PDM input valid data (in_pdm_data[0-N]) of multiple channels is obtained for double edge sampling. And the IP outputs valid data for multiple channels after a period of time. Each channel is distinguished by a synchronous signal (out_pcm_sync).

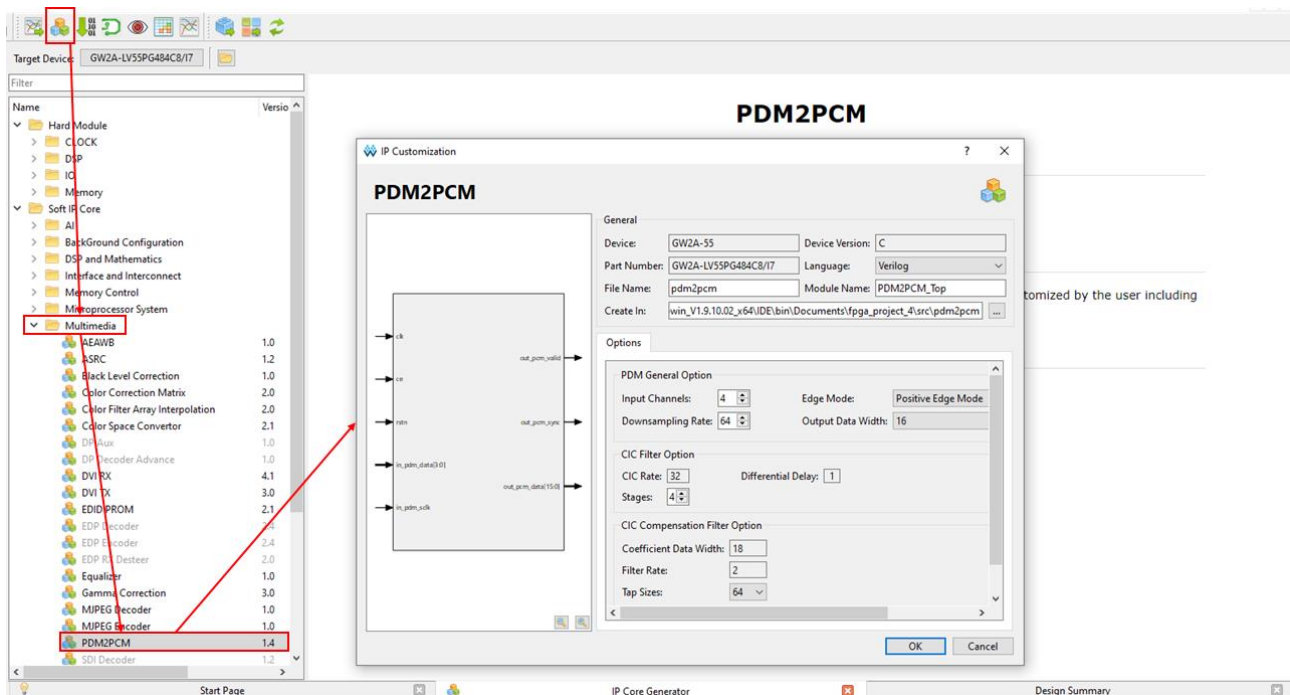
7 Call and Configuration

In Tools menu bar of the Gowin Software interface, it can start the IP Core Generator tool and complete PDM2PCM call and configuration.

1. Open IP Core Generator

After creating a new project, you can click the "Tools" button to open the IP Core Generator, as shown in Figure 7-1.

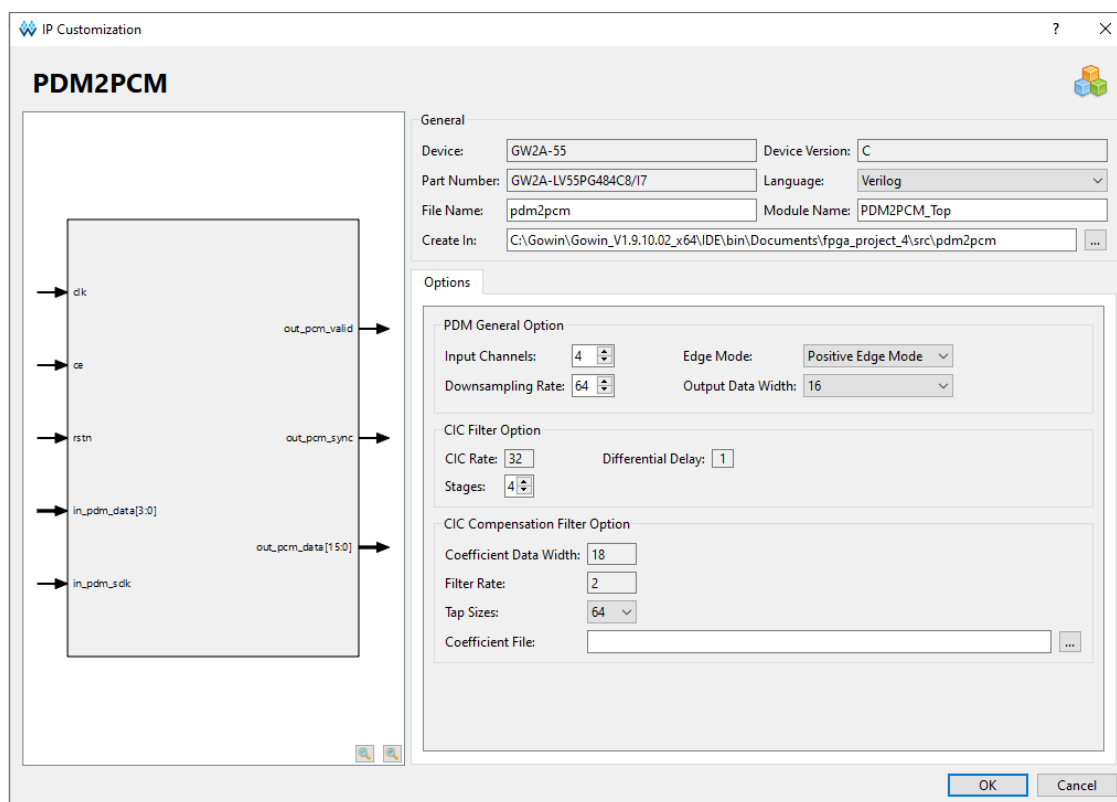
Figure 7-1 IP Core Generator GUI



2. Open PDM2PCM IP core

Click "Multimedia" and double click "PDM2PCM" to open the configuration interface, as shown in Figure 7-2.

Figure 7-2 PDM2PCM Configuration Interface



3. PDM2PCM Configuration

As shown in Figure 7-2, the "Module Name" option displays the top-level file name of the generated project, and the default is "EDID_PROM_Top". You can modify the name. The folder generated by the IP core is shown in "File Name", which contains the files required by PDM2PCM IP core, and the default is "pdm2pcm". You can modify the path. "Create In" displays the path of IP core folder. The default is "\project path\src\pdm2pcm". You can modify the path.

The IP configuration interface displays "PDM General Option", "CIC Filter Option" and "CIC Compensation Filter Option". Users can configure them as required. The user-defined options are shown in Table 7-1.

Table 7-1 User-defined Options

Option	Description
PDM General Option	Number of input channels
	PDM clock edge mode
	Downsampling rate
	Output data width
CIC Filter Option	Number of CIC Filter stages

Option	Description
CIC Compensation Filter Option	Tap sizes of the CIC Compensation Filter
	CIC Compensation Filter coefficient file

Note!

When loading a coefficient file using the CIC Compensation Filter Option, the coefficients are in decimal format. The range of the initial coefficients is from -2^{17} to $2^{17}-1$, with one number per line. The number of coefficients must match the Taps Size.

In the coefficient file, the data should be placed in the following position:

h_0
 h_1
 h_2
 ...
 h_{N-1}

All data is stored as decimal plain text.

The coefficients of the CIC Compensation Filter can be generated using the following MATLAB example:

```

R = 32;
N = 4;
T = 64;

M = 1;
order = T - 1;
fsPCM = 48000;
fpass = fsPCM*0.4536; % Pass band frequency
cic = dsp.CICDecimator(R,M,N); % CIC
cic_gain = 1/(cic.DecimationFactor*cic.DifferentialDelay)^cic.NumSections;
cic_comp = dsp.CICCompensationDecimator(cic,'DecimationFactor',2, ...
    'PassbandFrequency',fpass, 'DesignForMinimumOrder',false, ...
    'FilterOrder',order,'SampleRate',fsPCM*2); % Compensation
coeff = round(coeffs(cic_comp).Numerator*2^17);
dlmwrite(['cic_comp_coeff.txt'],coeff,'delimiter','\n')

```

In this script, R, N, and T correspond to the CIC Rate, Stages, and Tap Sizes parameters in the IP configuration, respectively.

The reference design also provides example coefficient files for different configurations. For more details, refer to the reference design.

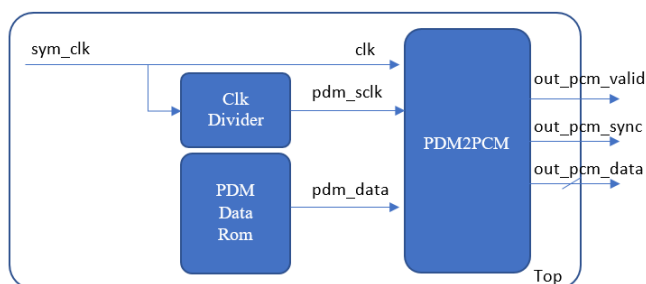
8 Reference Design

This chapter is intended to introduce the example and usage of PDM2PCM reference design. The PDM2PCM design example has only one module. Please refer to the [PDM2PCM reference design](#) for details.

The block diagram of the basic structure of the reference design is shown in Figure 8-1. In the design instance, the steps are as follows:

1. Store PDM data to ROM of PDM Data;
2. Output pdm_sclk through clock division module;
3. The output is obtained after PDM2PCM IP calculation.

Figure 8-1 Block Diagram of Reference Design



This design example allows for quick verification of the PDM2PCM functions. When the reference design is applied to board-level testing, the user must provide appropriate stimuli for the reference design, and signal observation can be performed using an on-chip logic analyzer or an oscilloscope.

In addition, the reference design provides CIC Compensation Filter coefficient files with different configurations in the docs\Compensation Filter Examples folder. For example, N4T64R32.txt corresponds to a configuration where the CIC Filter has 4 cascaded stages (Stages = 4), the CIC Compensation Filter length is 64 taps (Taps Size = 64), and the CIC decimation rate is 32 (CIC Rate = 32). Note that the CIC Rate is half of the total decimation factor.

