



Gowin RFFE IP

User Guide

IPUG785-1.0E,10/28/2021

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Revision History

Date	Version	Description
10/28/2021	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The purpose of Gowin RFFE IP User Guide is to help you quickly learn the features and usage of Gowin RFFE IP by providing descriptions of the functions, ports, timing, configuration, etc.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100](#), GW1N series of FPGA Products Data Sheet
- [DS117](#), GW1NR series of FPGA Products Data Sheet
- [DS102](#), GW2A series of FPGA Products Data Sheet
- [DS226](#), GW2AR series of FPGA Products Data Sheet
- [SUG100](#), Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
RAM	Random Access Memory
LUT	Look-up Table
RFFE	Radio Frequency Front End

Terminology and Abbreviations	Meaning
EMI	Electromagnetic Interference

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 RFFE Overview

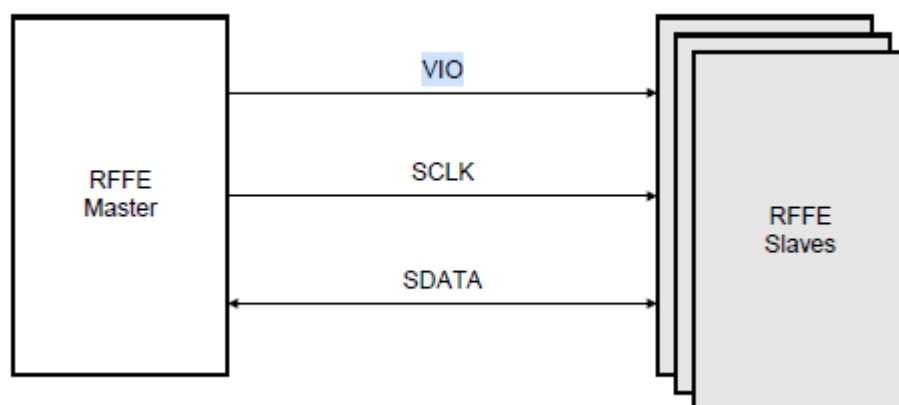
2.1 Physical Layer

Radio Frequency Front End, defined by MIPI, specifies the interface between the baseband and RF ICs with the intent to access the RF ICs registers using a single RFFE bus to minimize PCB and EMI. RFFE V1.0 features:

- Supports point-to-multipoint connectivity
- Supports fifteen slaves on a bus

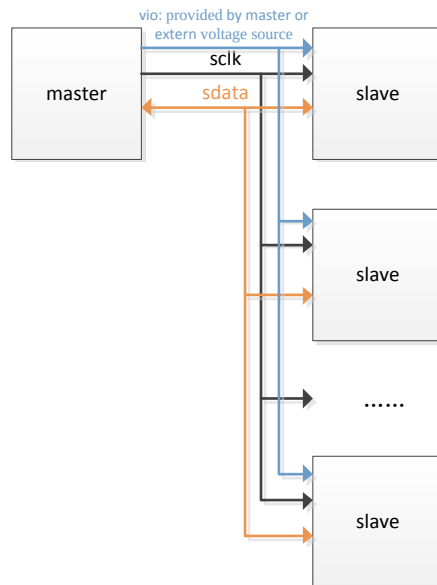
RFFE bus interface is as shown in Figure 2-1.

Figure 2-1 RFFE Bus Interface



- VIO: Bus supply voltage, provided by master or external reference voltage source.
- SCLK: Bus clock, provided by master,
- SDATA: Bus data, serial bidirectional.

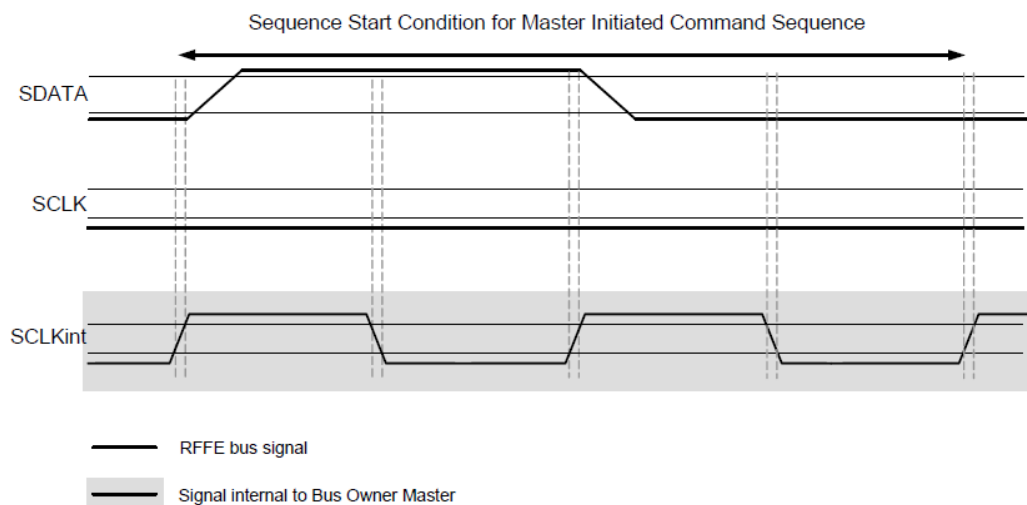
RFFE point-to multipoint topology is as shown in Figure 2-2.

Figure 2-2 Point-to-Multipoint Topology

2.2 Protocol Layer

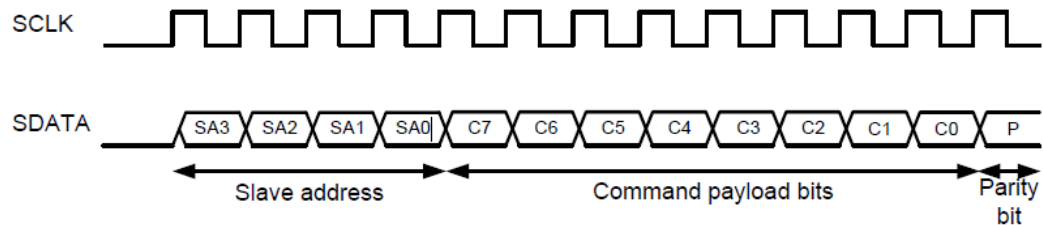
Master sends command sequence to access slaves on the bus. Command sequence is comprised of Sequence Start Condition (SSC), Command Frame, Data or Address Frame, and Bus Park Cycle, etc.

The SSC is used by the master to identify the start of a command sequence. The Master shall generate the SSC by driving SDATA to HIGH level for one SCLK period, then to LOW level for one SCLK period. The SSC must be followed by a command frame.

Figure 2-3 Sequence Start Condition

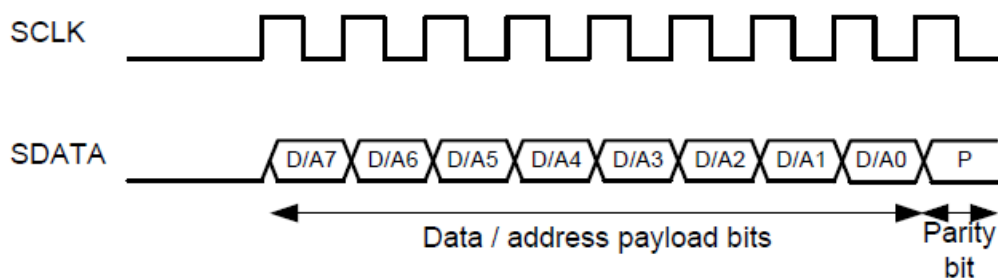
A Command Frame shall consist of a 4-bit slave address field, an 8-bit command payload field, and a single parity bit (the first 12 bits parity). The command frame structure is as shown in Figure 2-4.

Figure 2-4 Command Frame



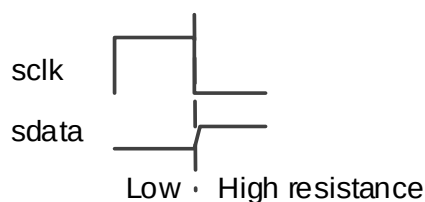
A data or address frame shall consist of eight data bits or eight address bits, and a single parity bit. A data or address frame structure is as shown in Figure 2-5.

Figure 2-5 Data or Address Frame



Bus Park Cycle is as shown in Figure 2-6. The device releasing SDATA shall drive the SDATA signal to a low level during the first half of the SCLK clock cycle. A device with ownership of SDATA shall initiate a Bus Park Cycle on SDATA at the end of a command sequence or when the device transfers control of SDATA to another device.

Figure 2-6 Bus Park Cycle



Command sequence supported by RFFE V1.0 is as shown in Figure 2-7.

Figure 2-7 Command Sequence

Mandatory Commands		Information		SSC		Command Frame		Data Frame	
M	S	Hex	Description	SSC		SA[3:0]	BC[3:0]	Address[7:0]	Up to 16 Bytes of Data with Parity Master must support up to 4 bytes
Y	O	00 0F	Extended Register Write	1	0	0 0 0 0	1 1 1 1	P	BP
		10	(Reserved)			0 0 0 1	0 0 0 0	P	Undefined
		11	(Reserved)			0 0 0 1	0 0 0 1	P	Undefined
		12	(Reserved)			0 0 0 1	0 0 1 0	P	Undefined
		13	(Reserved)			0 0 0 1	0 0 1 1	P	Undefined
		14	(Reserved)			0 0 0 1	0 1 0 0	P	Undefined
		15	(Reserved)			0 0 0 1	0 1 0 1	P	Undefined
		16	(Reserved)			0 0 0 1	0 1 1 0	P	Undefined
		17	(Reserved)			0 0 0 1	0 1 1 1	P	Undefined
		18	(Reserved)			0 0 0 1	1 0 0 0	P	Undefined
		19	(Reserved)			0 0 0 1	1 0 0 1	P	Undefined
		1A	(Reserved)			0 0 0 1	1 0 1 0	P	Undefined
		1B	(Reserved)			0 0 0 1	1 0 1 1	P	Undefined
		1C	(Reserved)			0 0 0 1	1 1 0 0	P	Undefined
		1D	(Reserved)			0 0 0 1	1 1 0 1	P	Undefined
		1E	(Reserved)			0 0 0 1	1 1 1 0	P	Undefined
		1F	(Reserved)			0 0 0 1	1 1 1 1	P	Undefined
Y	O	20 2F	Extended Register Read			SA[3:0]	BC[3:0]	P	Address[7:0] P BP Up to 16 Bytes of Data with Parity Master must support up to 4 bytes BP
O	O	30 37	Extended Register Write Long			SA[3:0]	BC[2:0]	P	Address[15:8] P Address[7:0] P Up to 8 Bytes of Data with Parity BP
O	O	38 3F	Extended Register Read Long			SA[3:0]	BC[2:0]	P	Address[15:8] P Address[7:0] P BP Up to 8 Bytes of Data with Parity BP
Y	O	40 5F	Register Write			SA[3:0]	Address[4:0]	P	Data[7:0] P BP
Y	O	60 7F	Register Read			SA[3:0]	Address[4:0]	P BP	Data[7:0] P BP
Y	O	80 FF	Register 0 Write			SA[3:0]	BC[0:0]	P BP	

Notes

All non-implemented Command Sequences and register accesses are ignored, resulting in a null response.

Nomenclature

BC = Byte Count

BP = Bus Park

M = Master

O = Optional

P = Parity

SA = Slave Address

Y = Mandatory

S = Slave

SSC = Sequence Start Condition

- Register 0 Write: Write data to register address 0 in the slave.
- Register Write: Write data to register addresses 0~31 in the slave, only 1 byte at a time.
- Register Read: Read data from register address 0~31 in the slave, only 1 byte at a time.
- Extended Register Write: Write data to register addresses 0~255 in the slave, and up to sixteen data bytes optional.
- Extended Register Read: Read data from register address 0~255 in the slave, and up to sixteen data bytes optional.
- Extended Register Write Long: Write data to register address 0~65535 in the slave, and up to eight data bytes optional.
- Extended Register Read Long: Read data from register address 0 to 65535 in the slave, and up to eight data bytes optional.

In the Extended register read and write operations, the address frame of the command sequence is the base address, and the internal incrementing is performed based on the base address in the slave.

Figure 2-8 shows the Register 0 Write command sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic one, and a seven bit word to be written to Register 0, and one-bit odd parity. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control to BusIDLE.

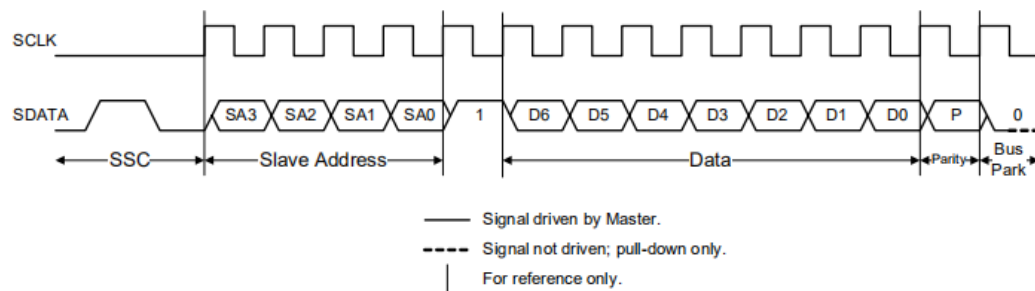
Figure 2-8 Register 0 Write Command Sequence

Figure 2-9 shows the Register Write command sequence. The Command Sequence starts with an SSC, followed by the Register Write Command Frame containing the Slave address, the data to be written, the target register address, and one-bit odd parity. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control to BusIDLE.

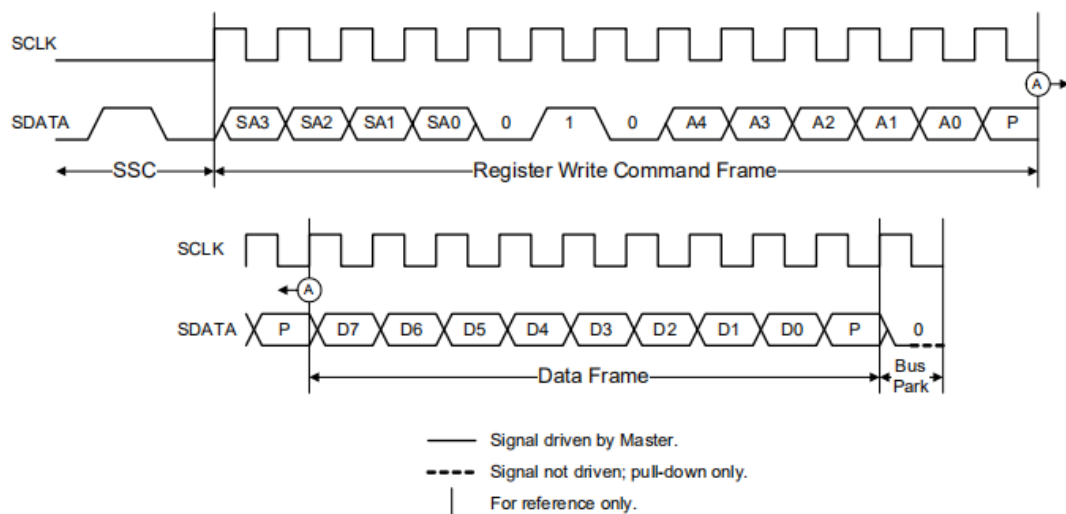
Figure 2-9 Register Write Command Sequence

Figure 2-10 shows the Register Read command sequence. The Command Sequence starts with an SSC, followed by Register Read Command Frame containing the Slave address, the data to be written, the target register address, and one-bit odd parity; then sends BusPark to transfer the SDATA bus control to the target slave. The slave sends the data frame containing eight bits data and one-bit odd parity to the master. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control to BusIDLE.

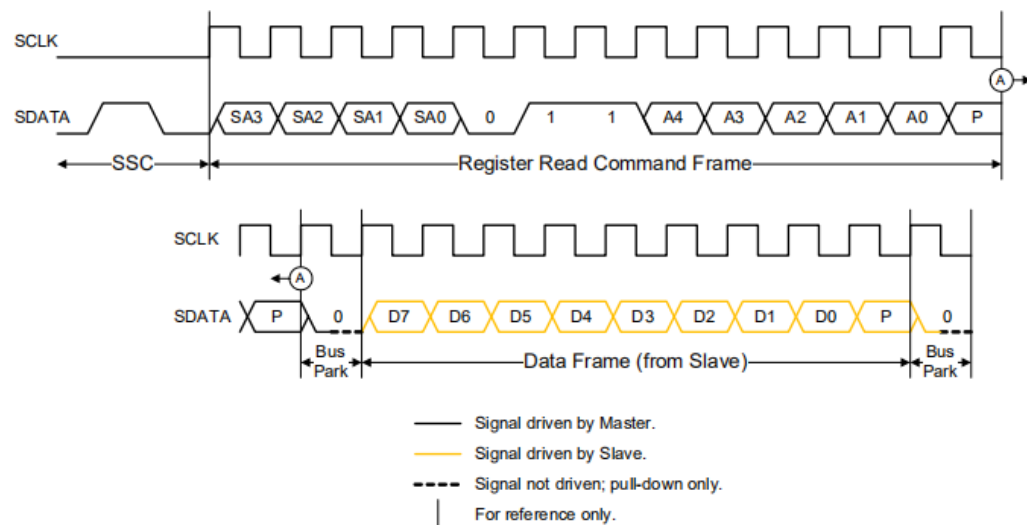
Figure 2-10 Register Read Command Sequence

Figure 2-11 shows the Extended Register Write command sequence. The Command Sequence starts with an SSC, followed by Extended Register Write Command Frame containing the Slave address, 4-bit binary 0000, BC[3:0], and one-bit odd parity; BC[3:0] = 0, which means the number of BYTE to be transferred is 1, and BC[3:0] = 15, which means the number of BYTE to be transferred is 16; then send the address frame containing the register address corresponding to the first BYTE. The internal address counter of the slave is incremented at this address. It should be noted that when the internal address counter reaches 0xFF, it will not start from address 0, and all subsequent BYTE data will overwrite 0xFF in turn; then confirm the number of data frames to send according to BC[3:0]. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control.

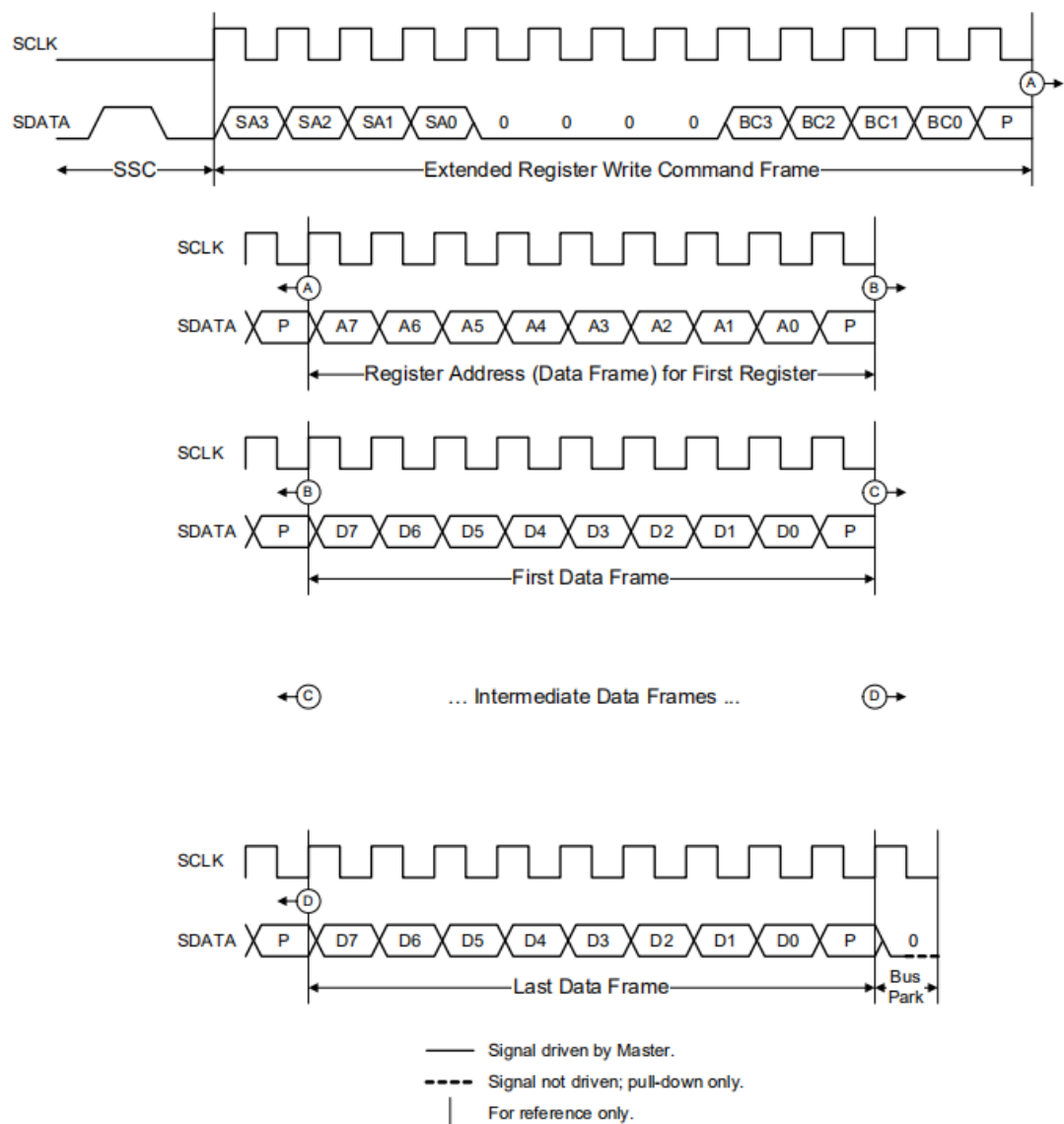
Figure 2-11 Extended Register Write Command Sequence

Figure 2-12 shows the Extended Register Read command sequence. The Command Sequence starts with an SSC, followed by Extended Register Read Command Frame containing the Slave address, 4-bit binary 0010, BC[3:0], and one-bit odd parity; BC[3:0] = 0, which means the number of BYTE to be read is 1, and BC[3:0] = 15, which means the number of BYTE to be read is 16; then send the address frame containing the register address corresponding to the first BYTE to read. The internal address counter of the slave is incremented at this address. It should be noted that when the internal address counter reaches 0xFF, it will not start from address 0, and all subsequent BYTE to read is 0xFF data; then confirm the

number of data frames to send according to BC[3:0]. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control.

Figure 2-12 Extended Register Read Command Sequence

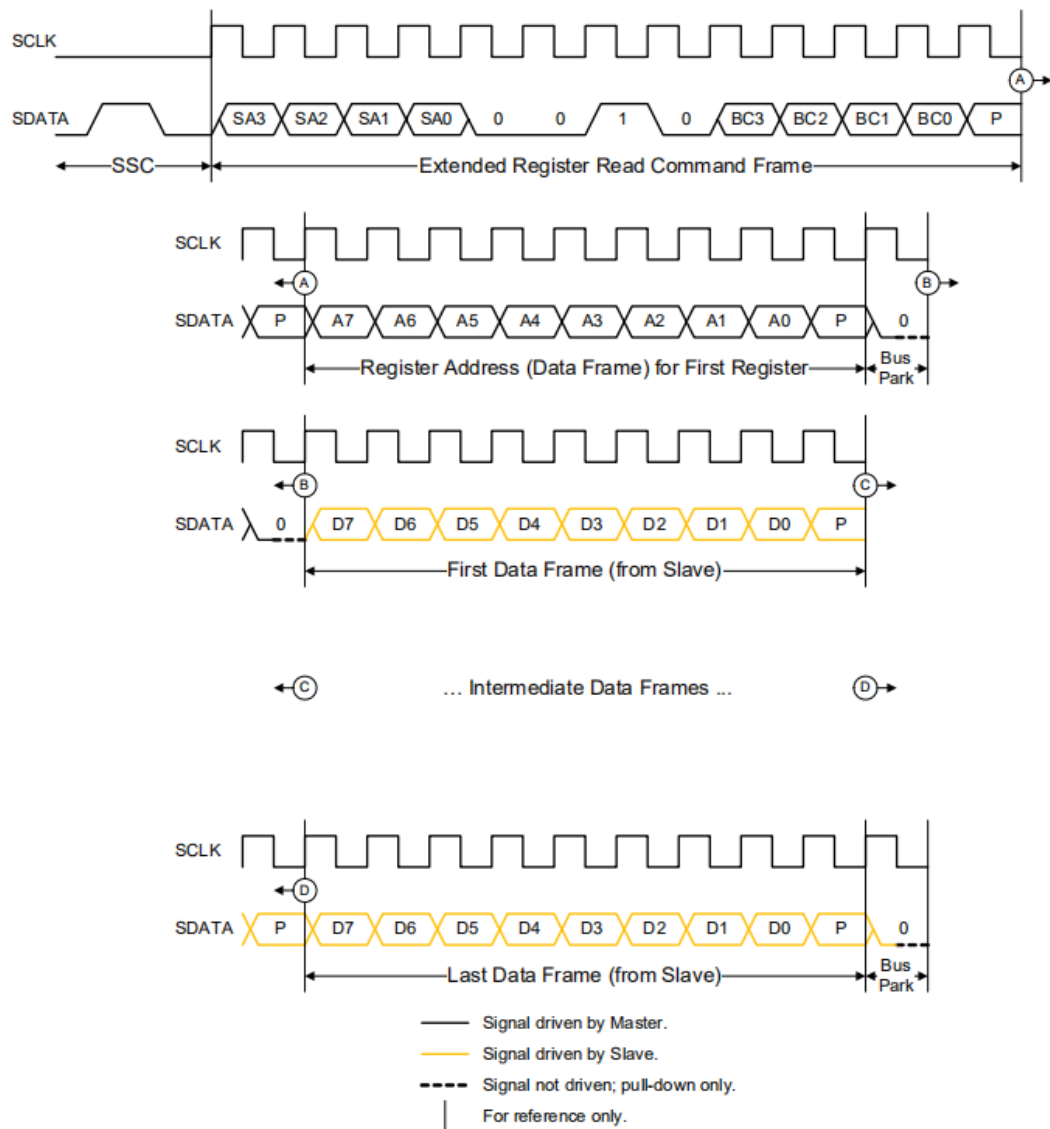


Figure 2-13 shows the Extended Register Write Long command sequence. The Command Sequence starts with an SSC, followed by Extended Register Write Long Command Frame containing the Slave address, 5-bit binary 00110, BC[2:0], and one-bit odd parity, where BC[2:0] = 0, which means the number of BYTE to be transferred is 1; BC[2:0] = 7, which means the number of BYTE to be transferred is 8; then send the higher and lower address frames containing the register address corresponding to the first BYTE. The internal address counter of the slave is incremented at this address. It should be noted that when the internal

address counter reaches 0xFFFF, it will not start from address 0, and all subsequent BYTE data will overwrite 0xFFFF in turn; then confirm the number of data frames to send according to BC[2:0]. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control.

Figure 2-13 Extended Register Write Long Command Sequence

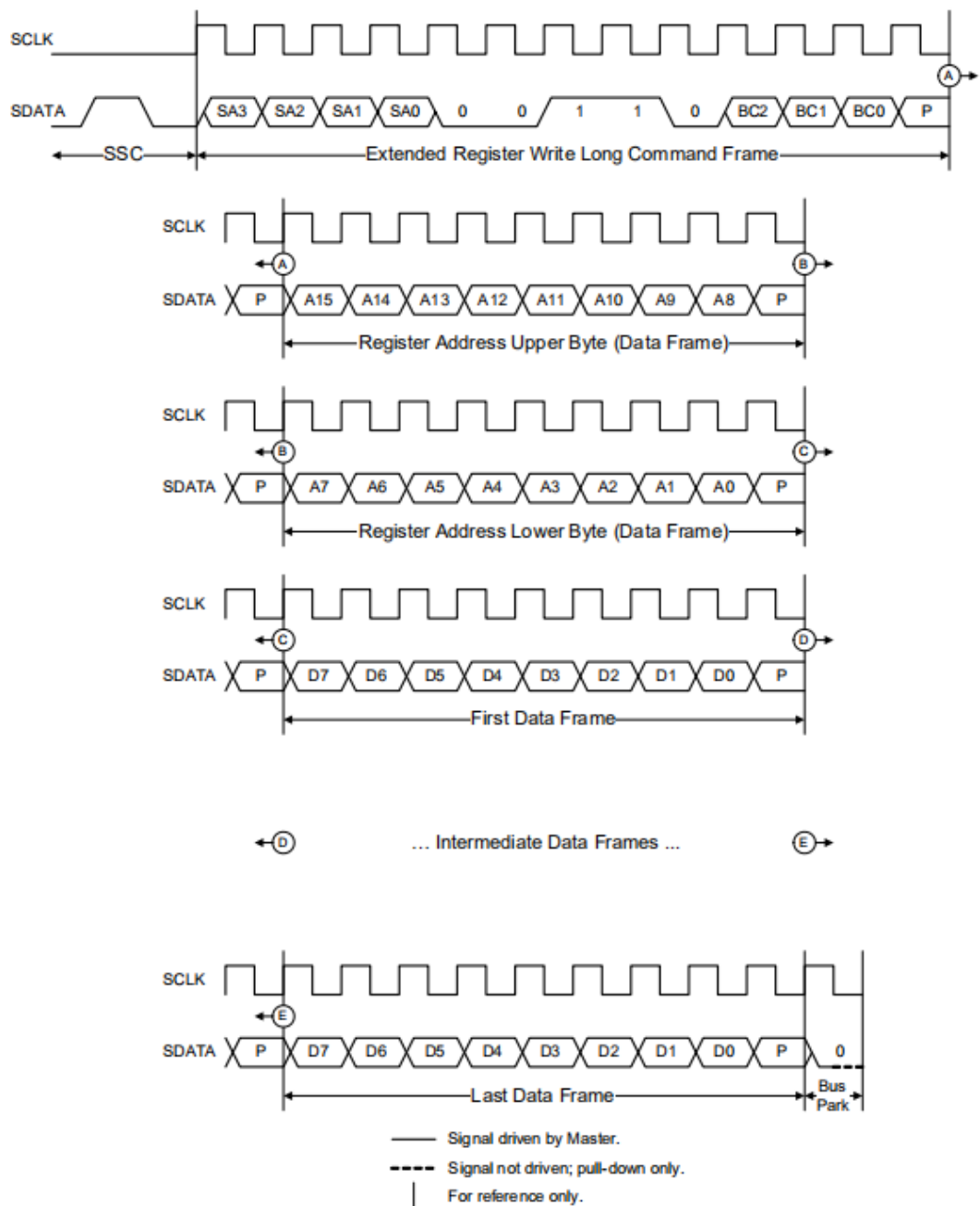
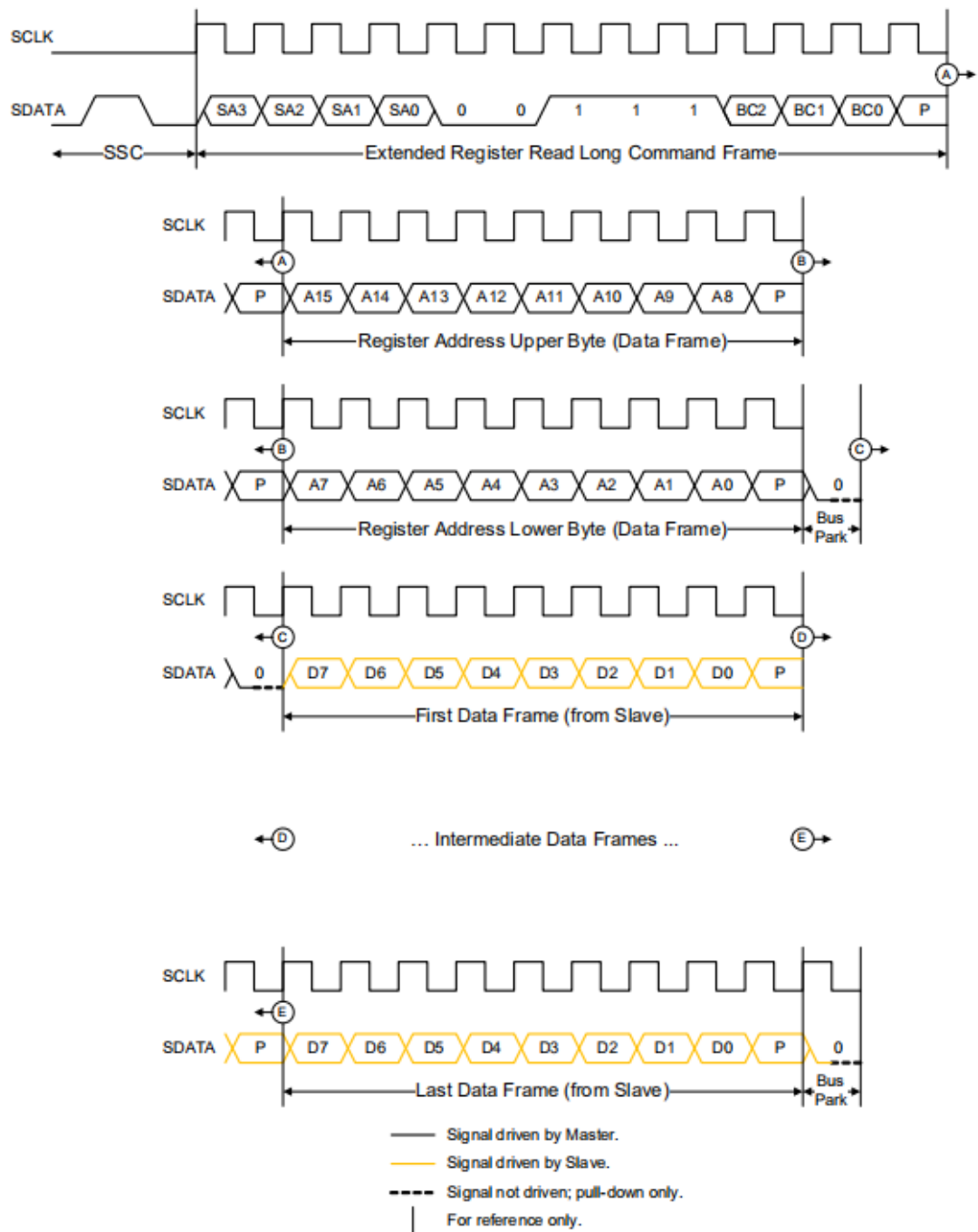


Figure 2-14 shows the Extended Register Read Long command sequence. The Command Sequence starts with an SSC, followed by

Extended Register Read Long Command Frame containing the Slave address, 5-bit binary 00111, BC[2:0], and one-bit odd parity; BC[2:0] = 0, which means the number of BYTE to be read is 1, and BC[2:0] = 8, which means the number of BYTE to be read is 8; then send the higher and lower address frames containing the register address corresponding to the first BYTE. The internal address counter of the slave is incremented at this address. It should be noted that when the internal address counter reaches 0xFFFF, it will not start from address 0, and all subsequent BYTE to read is 0xFFFF data; then confirm the number of data frames to send according to BC[2:0]. The Command Sequence ends with a Bus Park Cycle to transfer the SDATA bus control.

Figure 2-14 Extended Register Read Long command sequence



3 RFFE Master

RFFE Master IP supports all command sequences of RFFE V1.0, supports point-to-multipoint topology, can mount 15 slave devices, and you can modify the slave device ID on the bus by certain user logic + IP.

RFFE Master IP includes non-burst mode and burst mode; in non-burst mode, Extended Register Write/Read, Extended Register Write/Read Long operations can transfer only one BYTE; in burst mode, Extended Register Write/Read operations can transfer up to 16 bytes, and Extended Register Write/Read Long operations can transfer up to 8 bytes. The non-burst mode uses less resource compared to the burst mode, so you can choose as your requirements.

3.1 Port Description

The IO port of RFFE Master IP is shown in Figure 3-1 and Figure 3-2.

Figure 3-1 Non-burst Mode

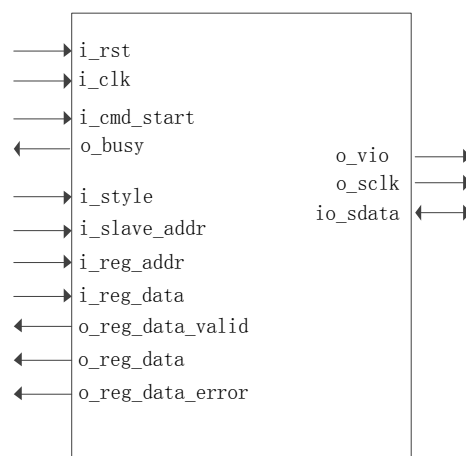
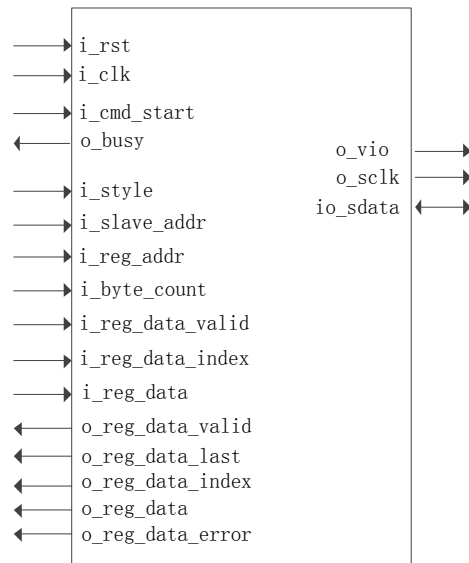


Figure 3-2 Burst Mode

For the details, you can refer to Table 3-1.

Table 3-1 IO Ports

Signal	I/O	Data Width	Description
<code>i_rst</code>	Input	1	Synchronous reset, active-high.
<code>i_clk</code>	Input	1	Working clock
<code>i_cmd_start</code>	Input	1	Command start, active-high; send command sequence only when <code>o_busy</code> is low and <code>i_cmd_start</code> is high.
<code>o_busy</code>	Output	1	Command sequence is being transmitted.
<code>i_style</code>	Input	3	Command type, <code>i_cmd_start</code> active-high. 0: Register Write, register address 0~31. 1: Register Read, register address 0~31. 2: Extended Register Write, register address 0~255. 3: Extended Register Read, register address 0~255. 4: Extended Register Write Long, register address 0~65535. 5: Extended Register Read Long, register address 0~65535. 6: Register 0 Write, register address 0. 7: reserve, invalid, will not respond even if <code>i_cmd_start</code> is high.
<code>i_slave_addr</code>	Input	4	Slave ID address, <code>i_cmd_start</code> active-high.
<code>i_reg_addr</code>	Input	16	Slave register address, <code>i_cmd_start</code> active-high.

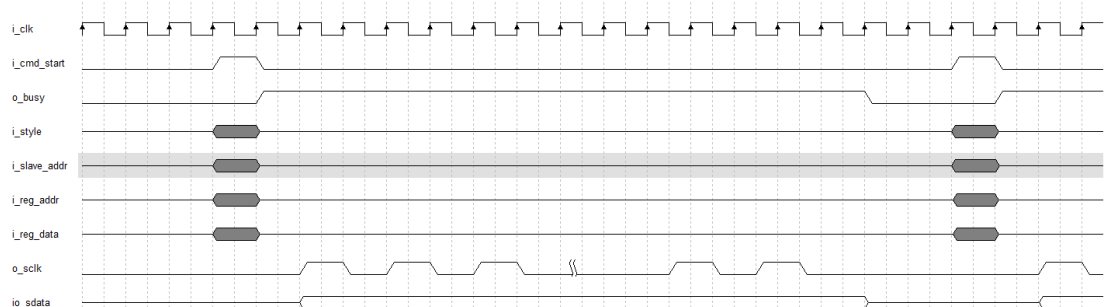
Signal	I/O	Data Width	Description
			Register Write& Register Read: Lower 5 bits, other bits are invalid. Extended Register Write& Register Read: Lower 8 bits, other bits are invalid. Extended Register Write Long& Extended Register Read Long: All 16 bits valid. Register 0 Write: All 16 bits invalid.
Burst mode (Check Burst Setting in Master)			
i_byte_count	Input	4	The number of BYTE, i_cmd_start active-high. Extended Register Write & Extended Register Read: Four bits valid, up to 16 bytes. Extended Register Write Long& Extended Register Read Long: Lower 3 bits valid, up to 8 bytes. Other instructions: Ignore this signal
i_reg_data_valid	Input	1	The validity of BYTE data writing to IP RAM, and ensure that data has been written to RAM before i_cmd_start is high.
i_reg_data_index	Input	4	The address of BYTE data writing to IP RAM, 0~15; if the instruction is Extended Register Write Long, then IP only sends address data between 0~7 in RAM.
o_reg_data_valid	Output	1	BYTE data read valid, active-high.
o_reg_data_last	Output	1	The last BYTE read valid, active-high.
o_reg_data_index	Output	4	Index, 0-15; indicate to read which BYTE.
o_reg_data	Output	8	Register data of slave read
o_reg_data_error	Output	1	Determines if there is a parity error in the read data; 1 means error. If it is ExtendedRead, the signal will be pulled up whenever there is a BYTE parity error.
Non-burst mode (Uncheck Burst Setting in Master)			
i_reg_data	Input	8	BYTE data written, i_cmd_start active-high.
o_reg_data_valid	Output	1	BYTE data read valid, active-high.
o_reg_data	Output	8	Register data read
o_reg_data_error	Output	1	Determines if there is a parity error in the read data; 1 means error.
RFFE physical layer			
o_vio	Output	1	RFFE interface supply voltage, pulled down only during IP reset.

Signal	I/O	Data Width	Description
o_sclk	Output	1	Serialclk, the output serial clock is determined by the value of Rffe Clock Setting, and the output frequency is the frequency of i_clk divided by Rffe Clock Rate Setting, and Rffe Clock Rate Setting only supports even numbers.
io_sdata	Inout	1	Serial data

3.2 Timing Description

Figure 3-3 shows write operation of burst mode.

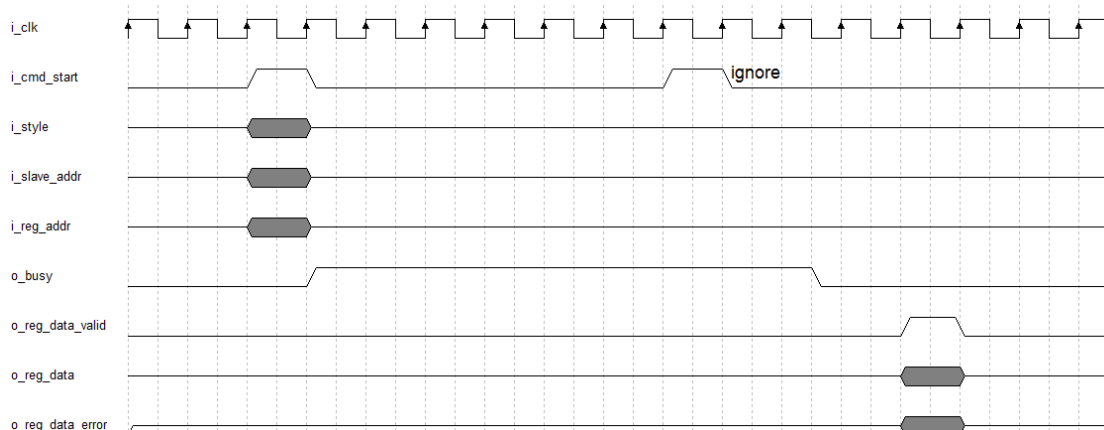
Figure 3-3 Write Operation in Non-burst Mode



When i_cmd_start is high and o_busy is low, the command sequence is valid; i_style, i_slave_addr, i_reg_addr, and i_reg_data can be sampled. i_slave_addr corresponds to the slave ID to be accessed, i_reg_addr corresponds to the register address to be accessed, and i_reg_data corresponds to the data to be written.

Figure 3-4 shows read operation of non-burst mode.

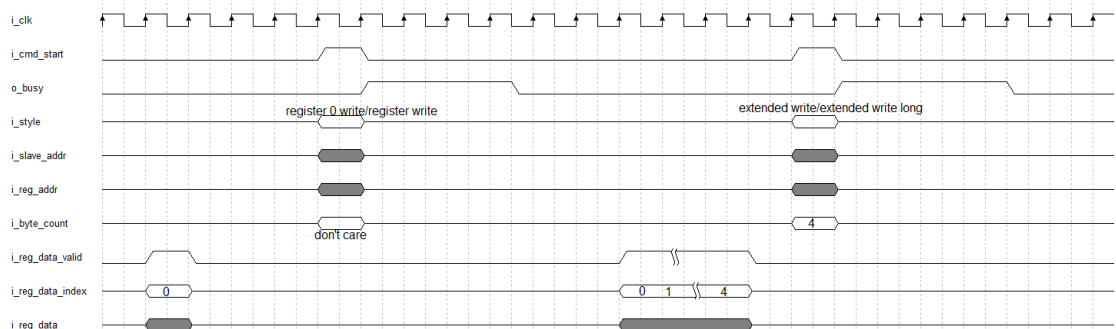
Figure 3-4 Read Operation in Non-burst Mode



When `i_cmd_start` is high and `o_busy` is low, the command sequence is valid; `i_style`, `i_slave_addr`, `i_reg_addr`, and `i_reg_data` can be sampled. `i_slave_addr` corresponds to the slave ID to be accessed, `i_reg_addr` corresponds to the register address to be accessed, and `i_reg_data` corresponds to the data to be read.

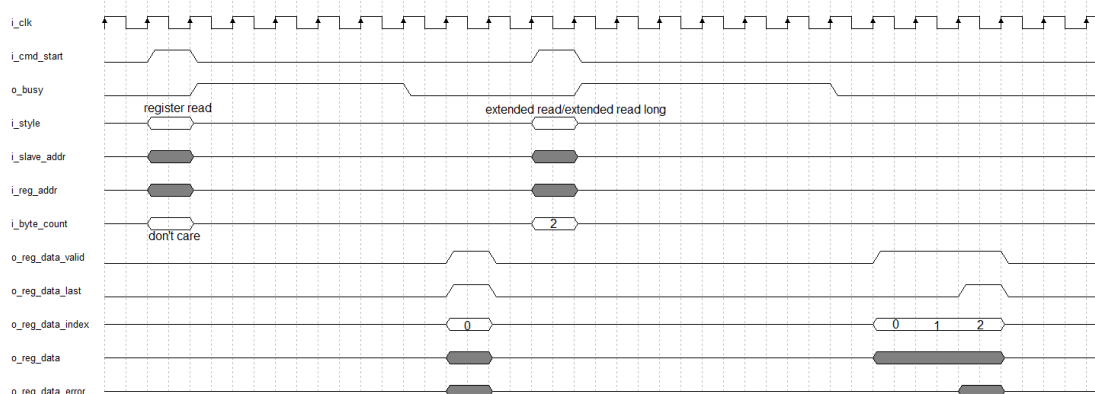
Figure 3-5 shows write operation of burst mode.

Figure 3-5 Write Operation Burst Mode



Before the command sequence is valid (`i_cmd_start` is high and `o_busy` is low), the data to be sent is written to the internal RAM, and `i_reg_data_index` corresponds to the address of the internal RAM. Until the command sequence is valid, the data in the internal RAM is read and sent according to the command. As shown in Figure 3-5, before the command is valid, one byte data is written to address 0 of the internal RAM, and after the command is valid, the internal RAM is addressed and the data is sent according to the command. For example, for Register 0 Write and Register Write operations, one byte data is written to address 0 of internal RAM before the command is valid, and after the command is valid, address 0 data in RAM is sent because Register 0 Write and Register Write are both sending one byte data; for Extended Write and Extended Write long operations, the data to be sent is written to the internal RAM before the command is valid, and after the command is valid, the data in the internal RAM read by `i_byte_count` is sent.

Figure 3-6 shows read operation of burst mode.

Figure 3-6 Read Operation Burst Mode

For the read operation in burst mode, when the command sequence is valid, the corresponding register data of the slave device is read according to the command, and the Register Read reads only one BYTE data each time; Extended Read can access 1~16 BYTE data in succession from the register address of the slave, and Extended Read Long can access 1~8 BYTE data in succession from the register address of the slave.

3.3 Resource Utilization

Table 3-2 RFFE Master IP Resource Utilization

Device Series	Mode	Device	Resource Utilization	Remarks
GW2A	Non-burst Mode	Register	169	—
		LUT	160	
		ALU	6	
		DSP	0	
		BSRAM	0	
	Burst Mode	Register	232	
		LUT	204	
		ALU	12	
		DSP	0	
		BSRAM	1	

4 RFFE Slave

RFFE Slave IP contains a write interface and a read interface. Master can write register data to the Slave via write interface and read register data from the Slave via read interface.

Note!

Read operation interface can be checked or unchecked, if unchecked, it can reduce Slave IP resources.

4.1 Port Description

For the IO details, you can refer to Table 4-1.

Table 4-1 IO Description

Signal	I/O	Data Width	Description
i_clk	Input	1	The working clock i_clk should be at least 4 times higher than i_sclk.
i_slave_addr	Input	4	Slave address
o_cmd_err	Output	1	Command frame parity error; high indicates parity check error.
RFFE physical layer			
i_vio	Input	1	Slave enable interface If it is low, IP can not work.
i_sclk	Input	1	Serial clk
io_sdata	Inout	1	Serial data
Read operation interface (Check Read Support in Slave)			
o_rd_en	Output	1	Read enable signal, active-high.
o_rd_addr	Output	16	Read register address; use o_rd_en to indicate whether the signal is valid or not.
i_rd_data	Input	8	The data returned from the register address needs

Signal	I/O	Data Width	Description
			to be put into the data bus at the next clock cycle when o_rd_en is high.
o_rd_addr_frame_err	Output	2	In read operation, address frame parity error. High indicates there is an error.
Write operation interface			
o_wr_en	Input	1	Write enable signal, active-high.
o_wr_addr	Output	16	Write register address; use o_wr_en to indicate whether the signal is valid or not.
o_wr_data	Output	8	Write register data; use o_wr_en to indicate whether the signal is valid or not.
o_wr_data_err	Output	1	Register data parity error; high indicates there is an error.
o_wr_addr_frame_err	Output	2	In write operation, address frame parity error. High indicates there is an error.

4.2 Timing Description

Figure 4-1 shows the write operation of Slave.

Figure 4-1 Slave Write Operation

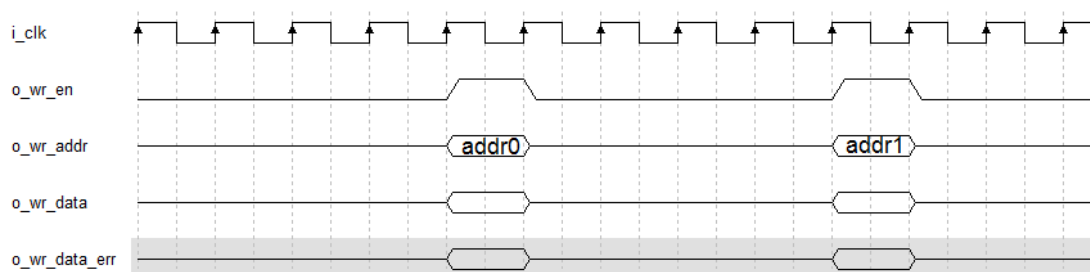
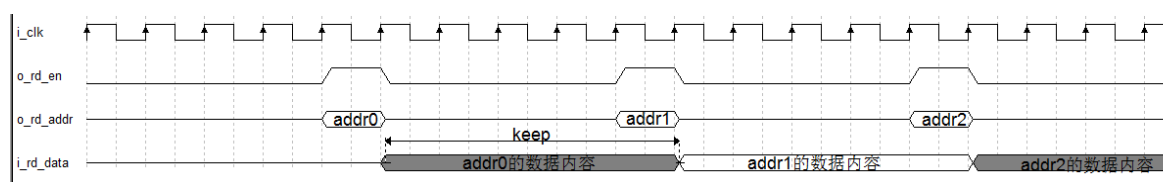


Figure 4-2 shows the read operation of Slave.

Figure 4-2 Slave Read Operation



In read operation, it should be noted that the read data needs to hold for some time, and it is recommended to hold it until the next read operation.

4.3 Resource Utilization

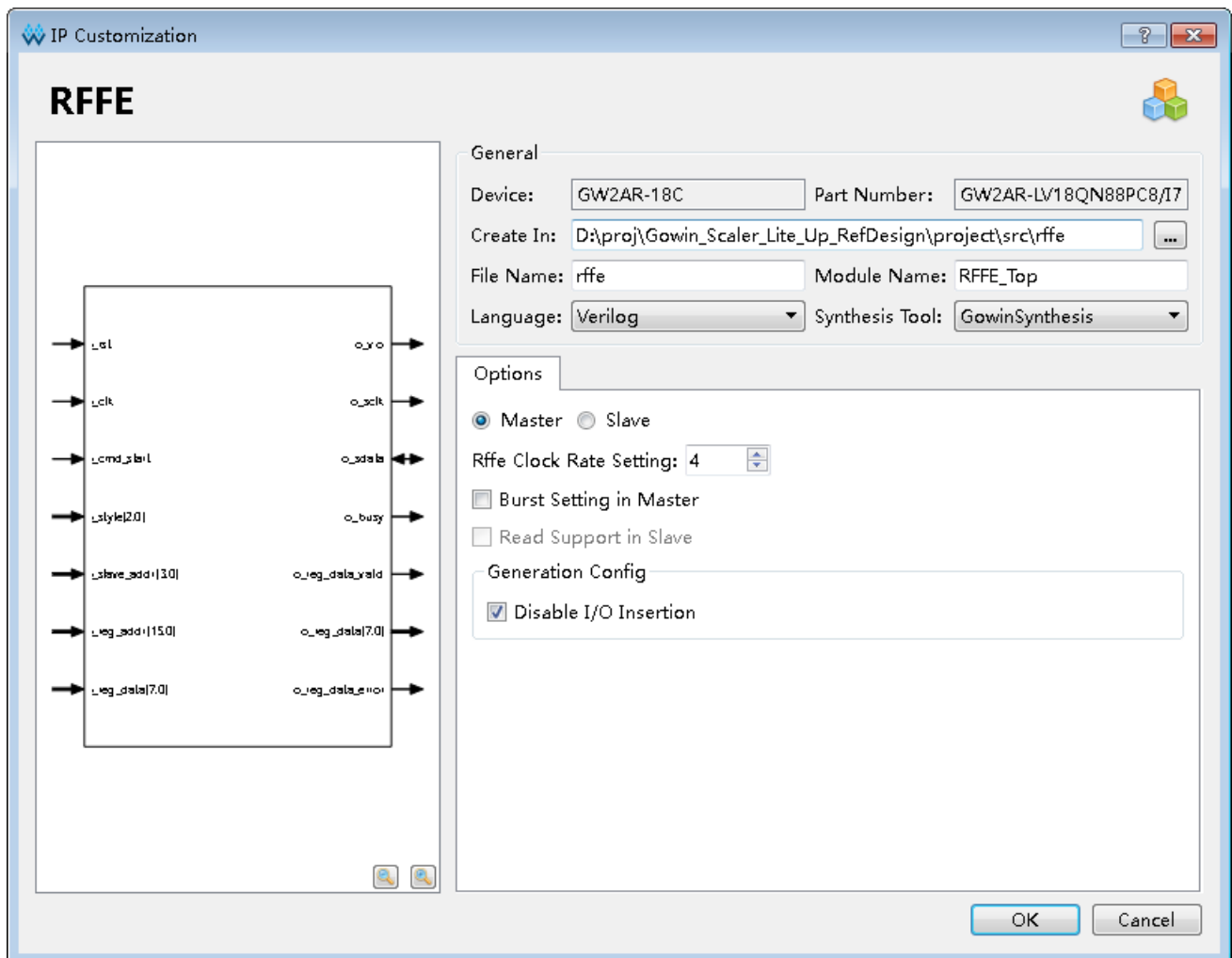
Table 4-2 RFFE Slave IP Resource Utilization

Device Series	Mode	Device	Resource Utilization	Remarks
GW1N	Only Write	Registers	144	—
		LUT	140	
		ALU	8	
		DSP	0	
		BSRAM	0	
	Write & Read	Registers	230	
		LUT	258	
		ALU	32	
		DSP	0	
		BSRAM	0	

5 RFFE IP Configuration Description

There are four configuration options as shown below.

Figure 5-1 GUI



- Master or Slave: Select a master or slave device.

- Burst Setting in Master: When checked, Master selects burst mode, 1~16 bytes optional; unchecked, single byte.
- Rffe Clock Rate Setting: It can only be an even number and is used to configure the frequency of the RFFE serial clock sclk, which is equal to the IP system clock divided by the Rffe Clock Rate Setting.
- Read Support in Slave: When checked, it supports read operation from the master to the slave; if unchecked, only write operation can be performed on the slave.

