



Gowin PSRAM Memory Interface HS IP

User Guide

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03/04/2021	1.1E	Chapter 5 Port List updated.
06/30/2021	1.2E	Shift delay added.
11/22/2024	1.3E	● Descriptions of Data Mask (data_mask) added. ● "Help" option removed.
07/04/2025	1.4E	● Address port description updated. ● Descriptions of 3.2 Operating Frequency and Bandwidth Efficiency updated. ● Descriptions of 3.3 Resource Utilization updated. ● IP manual name updated from Gowin PSRAM Memory Interface HS & HS 2CH IP to Gowin PSRAM Memory Interface HS IP.
03/09/2026	1.5E	The cmd_rdy port and its usage description added.

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1 About This Guide

1.1 Purpose

Gowin PSRAM Memory Interface HS IP user guide includes the product overview, features and performance, functional description, port description, timing description, configuration and call, reference design, etc. The guide helps you learn the feature and usage of Gowin PSRAM Memory Interface HS IP. The IP supports both single-channel and dual-channel configurations. The usage is essentially the same for both. This manual primarily focuses on single-channel usage, with additional notes of dual-channel. The software screenshots and the supported products listed in this manual are based on Gowin Software V1.9.11.03. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com.cn:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
2CH	2 Channels
GSR	Global System Reset
HS	High Speed
IP	Intellectual Property
LUT	Look-up Table
PSRAM	Pseudo Static Random Access Memory
RAM	Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

Gowin PSRAM Memory Interface HS IP is a common used PSRAM interface IP, in compliance with PSRAM standard protocol. The IP includes the PSRAM MCL (Memory Controller Logic) and the corresponding PHY (Physical Interface) design. Gowin PSRAM Memory Interface HS IP provides you a generic command interface to connect with the PSRAM chip for data access.

Table 2-1 Gowin PSRAM Memory Interface HS IP

Gowin PSRAM Memory Interface HS IP	
Logic Resource	Please refer to Table 3-1.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8Beta and above)

Note!

For the devices supported, you can click [here](#) to get the information.

3 Features and Performance

3.1 Features

- Supports PSRAM W955D8MKY-6I part number.
- Supports memory data path widths of 8, 16, 24, and 32 bits
- Supports memory chip with x8 data width
- Programs 16, 32, 64 or 128 burst lengths
- The clock rate is 1:2
- The initial latency is six clock cycles
- Supports a fixed latency mode
- Supports a power off option
- Configurable drive strength
- Configurable self-refresh area
- Configurable refresh rate
- Supports single-channel and two-channel operation modes

3.2 Operating Frequency and Bandwidth Efficiency

The data rate and efficiency of Gowin PSRAM Memory Interface HS IP supports:

- The IP supports a maximum operating frequency of up to 166 MHz; however, the actual maximum frequency may vary depending on the performance of the FPGA device.
- 128 burst lengths with a bandwidth efficiency of 74 percent.
- 64 burst lengths with a bandwidth efficiency of 61 percent.
- 32 burst lengths with a bandwidth efficiency of 44 percent.
- 16 burst lengths with a bandwidth efficiency of 28 percent.

3.3 Resource Utilization

Gowin PSRAM Memory Interface HS IP employs the Verilog language, which can be used in LittleBee and Arora family devices, etc. Table 3-1 presents an overview of the resource utilization. For the applications on other GOWINSEMI FPGA devices, please see the later release information.

Table 3-1 Resource Utilization

DQ_WIDTH	LUT	REGs	I/O	f _{MAX}	Device Series	Speed Level
16(x8)	1004	620	29	333Mbps	GW1NR-9	C6/I5

Note!

In Table 3-1, the user address width of Gowin PSRAM Memory Interface HS IP is 21 bits, PSRAM WITDH is x8, and burst length is 128; and the resource utilization will be increased in the two-channel PSRAM IP.

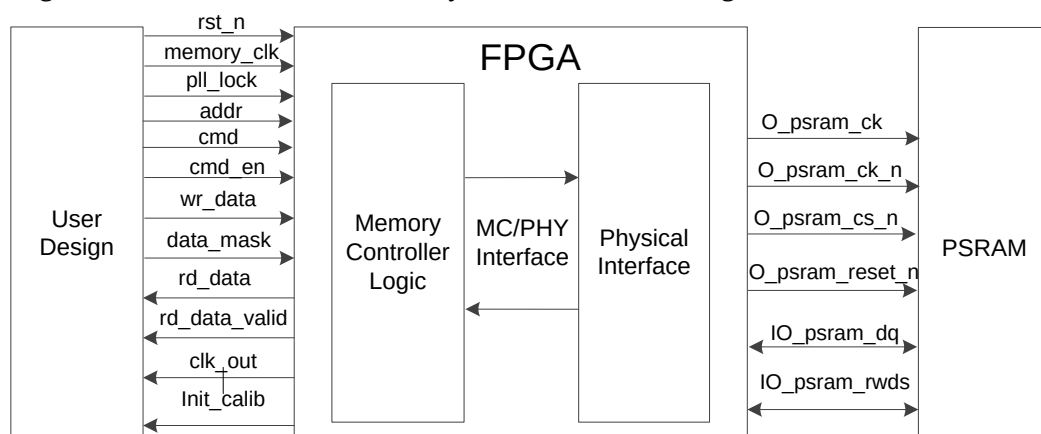
4 Functional Description

4.1 Structure

As shown in Figure 4-1, Gowin PSRAM Memory Interface HS IP mainly includes Memory Controller Logic, Physical Interface, etc.

The User Design module in Figure 4-1 is the module connected to the external PSRAM chip in FPGA.

Figure 4-1 Gowin PSRAM Memory Interface HS IP Diagram

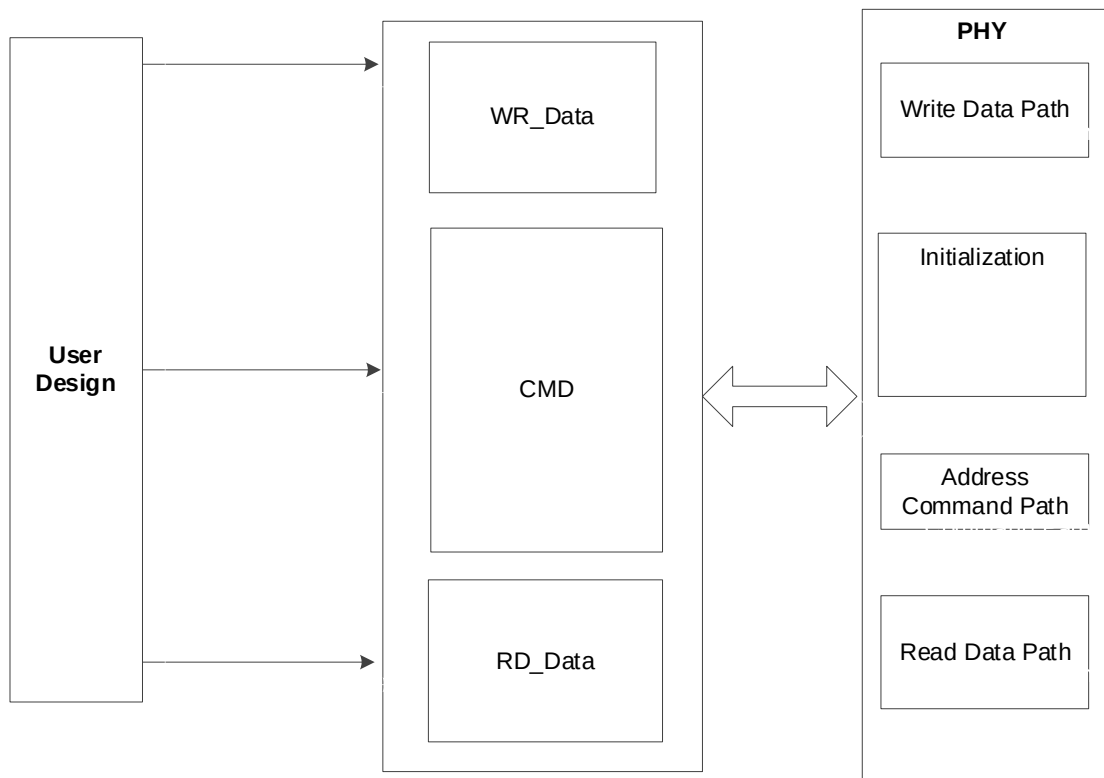


4.2 Memory Controller Logic

Memory Controller Logic is the logic module of Gowin PSRAM Interface HS IP, which locates between User Design and PHY. The Memory Controller Logic receives the command, address, and data from the user interface and stores them in logical order.

The write, read and other commands sent by the user are sorted and reorganized in Memory Controller Logic to combine a data format that complies with the PSRAM protocol. Meanwhile, when the Memory Controller Logic writes data, the data will be reorganized and cached to meet the initial delay value between the command and the data. When the Memory Controller Logic reads the data, the data will be sampled and reorganized to be the correct one.

The PSRAM Memory Controller includes the CMD unit, the WR_Data unit, the RD_Data unit, etc. The main structure is shown in Figure 4-2.

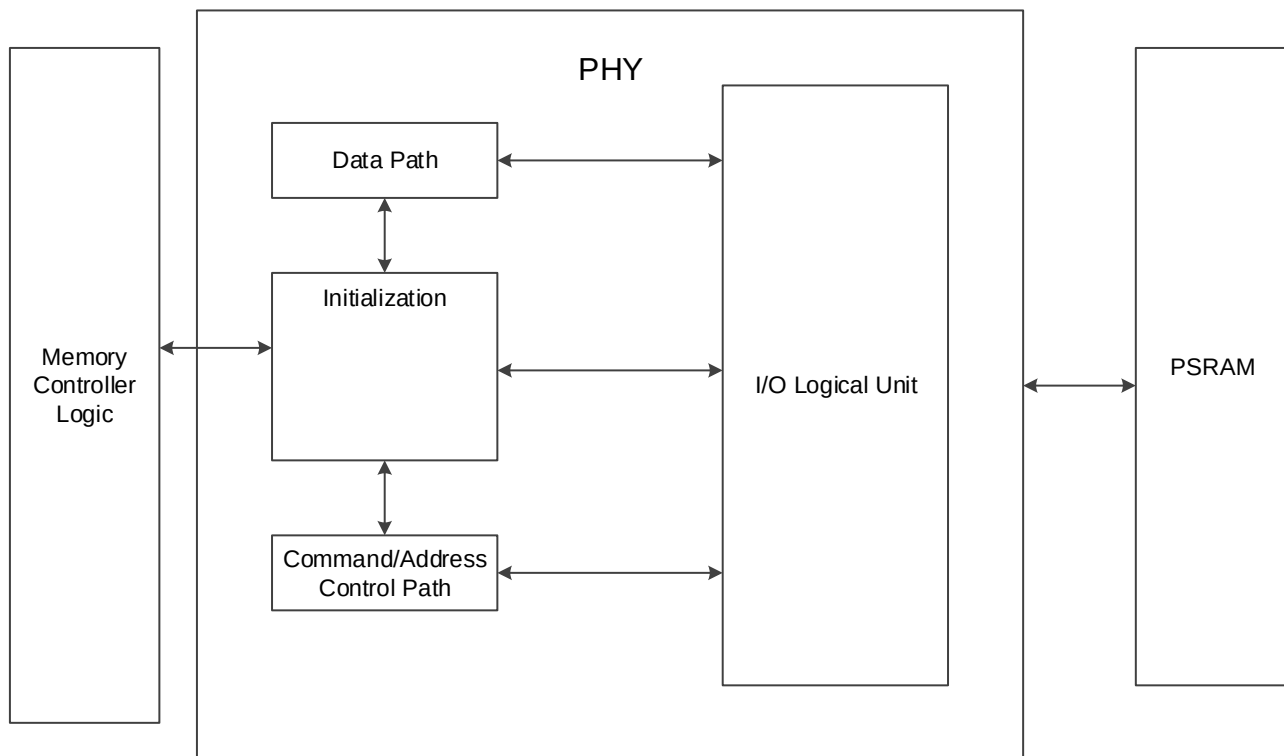
Figure 4-2 PSRAM Memory Controller Logic Basic Structure

4.3 PHY

The PHY provides the physical layer definition and interface between Memory Controller Logic and the external PSRAM. It receives the command address and data from the Memory Controller Logic and provides the PSRAM interface with signals that meet the timing and sequence requirements.

The structure of the PHY includes four modules: initialization module, data path, command/address control path and I/O logic module, as shown in Figure 4-3.

Figure 4-3 PSRAM PHY Structure



4.3.1 Initialization Unit

The initialization module is mainly used for the initialization and read-calibration after power on. After all initialization and read-calibration are finished, the signal "init_calib" will become high to indicate the completion of the entire initialization.

Power-on Initialization

According to the PSRAM protocol standard, it needs to initialize the PSRAM after power on. This includes the reset, mode register configuration, and read calibration.

4.3.2 Data Path Unit

Data path includes write data path and read data path.

4.3.3 Command/Address Control Path Unit

The command/address control path is a single pass that receives the command and address signal sent by the Memory Controller Logic and cooperates with the data path to process the write and read data delay parameters and sends the commands to the I/O logic module.

4.3.4 I/O Logic Unit

The Logic I/O module is mainly used to convert the clock domain of the data, command, and address signals received from the data path and command/address path.

4.4 Major Functions

The functions of the PSRAM Memory Interface HS IP are as follows:

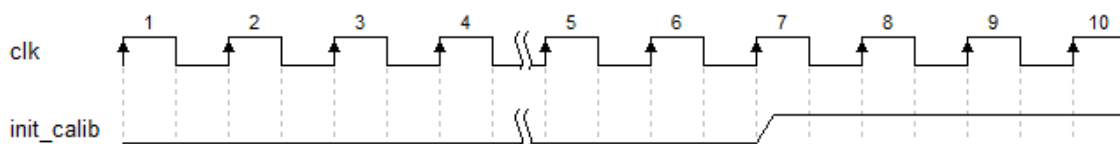
- Initialize the PSRAM chip
- Send the addresses and commands
- Write data
- Read data

4.4.1 Initialization

PSRAM must be read calibrated to perform normal write and read operations. Therefore, after power on, PHY performs initialization read calibration operation on PSRAM and returns to "init_calib" after initialization completion. Single channel PSRAM IP initializes two PSRAMs at the same time, while two-channel IP initializes two PSRAM respectively and sends two initialization completion signals to users respectively.

The completion signal is returned to the user after the initialization is completed, as shown in Figure 4-4.

Figure 4-4 Initialization Completion Signal Timing Diagram



4.4.2 Send Addresses and Commands

You can send operation commands and addresses through the addr, cmd, and cmd_en ports.

- The addr serves as the address data port. The IP design adopts bit-width extension to increase bandwidth. When multiple PSRAM chips are used, the IP treats them as a single PSRAM for access. Users do not need to consider address bit width changes when selecting one or multiple PSRAM chips. The address of the PSRAM chips supported by this IP is a word address, meaning each address stores a word length (16 bits = 2 bytes). For example, when the IP is configured in single-channel mode, it drives two PSRAM chips, and each address will store 4 bytes. The address length used for a single burst read or write is half of the burst length. For continuous address write/read operations, the address increments by burst length/2 between successive operations.
- cmd serves as the command data interface.
- cmd_en serves as the enable signal of the address and command, active high.
- The operation mode of two-channel PSRAM HS IP and single-channel PSRAM HS IP is the same, but the command and address of the two-channel PSRAM HS IP are independent, and control signals need to be given respectively.

In the application, a mapping relationship exists between the address

bus of user interface and the physical memory ROW, Upper Column, and Lower Column. In this design, it is in ROW-Upper Column-Lower Column order. The addressing scheme is as shown in Figure 4-5. In the application, you only need to give the address as needed, and do not need to concern about the mapping relationship.

Figure 4-5 Addressing Scheme in Row-Column Order



The commands sent by users through the cmd port are as shown in Table 4-1.

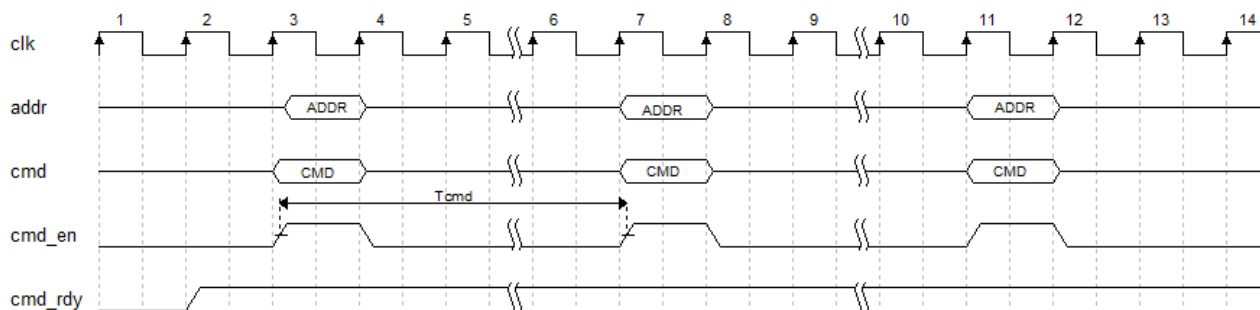
Table 4-1 cmd

Command	cmd
Read	1'b0
Write	1'b1

At the user interface, the timing between the command, address, and enable signals is as shown in Figure 4-6.

When the cmd_en is high, the cmd and the addr are valid at this time.

Figure 4-6 Command, Address, and Enable Signal Timing (1)



In applications, the two commands (write-read/read-write/write-write/read-read) interval must satisfy the minimum interval period (the interval period of T_{cmd} shown in Figure 4-8). That is, when the burst length is 16, the command interval is at least 14 clock cycles; when the burst length is 32, the command interval is at least 18 clock cycles; when the burst length is 64, the command interval is at least 26 clock cycles; when the burst length is 128, the command interval is at least 42 clock cycles, as shown in Table 4-2.

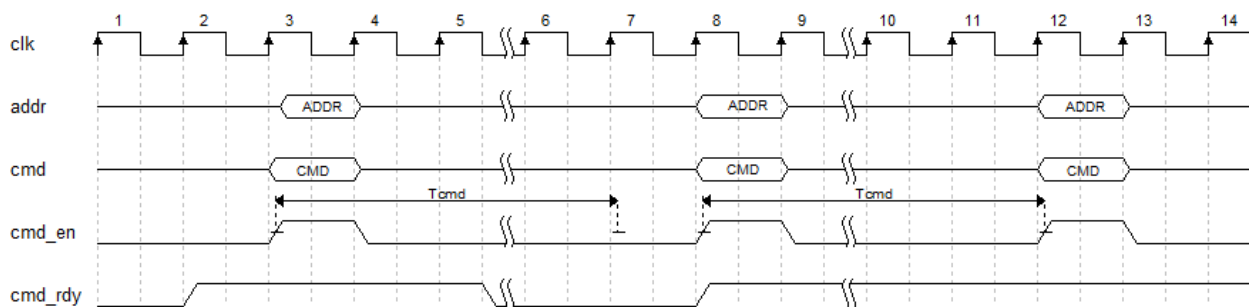
Table 4-2 Relationship between T_{cmd} Cycle and Burst Length

Burst Length	T_{cmd} (interval before two commands, regardless of read or write)
128	42 user clocks
64	26 user clocks
32	18 user clocks

Burst Length	Tcmd (interval before two commands, regardless of read or write)
16	14 user clocks

A write command is written by asserting `cmd_en`. In addition to meeting the `Tcmd` interval requirement, `cmd_rdy` must also be at logic 1. After the `Tcmd` interval counter expires, `cmd_rdy` is checked. If `cmd_rdy` is at logic 1, `cmd_en` can be asserted high; otherwise, the assertion of `cmd_en` must be delayed until `cmd_rdy` becomes high. The timing is shown in the figure below.

Figure 4-7 Command, Address, and Enable Signal Timing (2)



4.4.3 Write Data

You can send the data to Gowin PSRAM Memory Interface HS IP through the user ports of `wr_data` and `data_mask`, etc. The write data will be sent to the PSRAM after being processed.

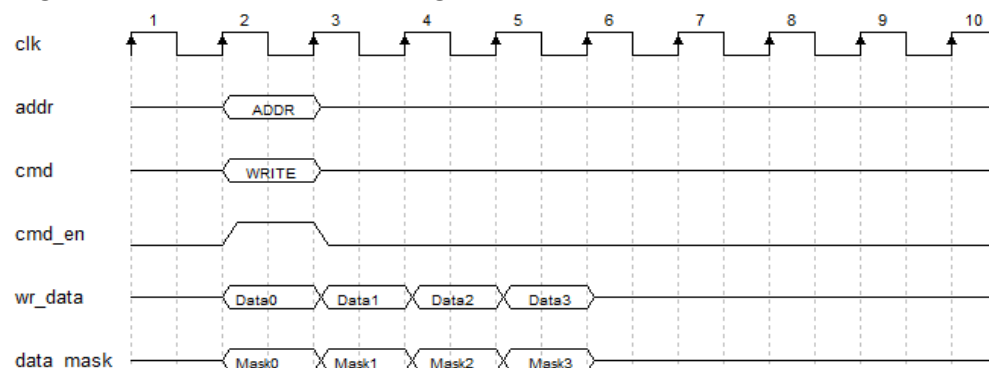
- The `wr_data` is a write data port.
- The `data_mask`^[1] is a write mask port.

Note!

^[1]For more information on the use of `data_mask`, you can see [Data Mask \(data_mask\)](#).

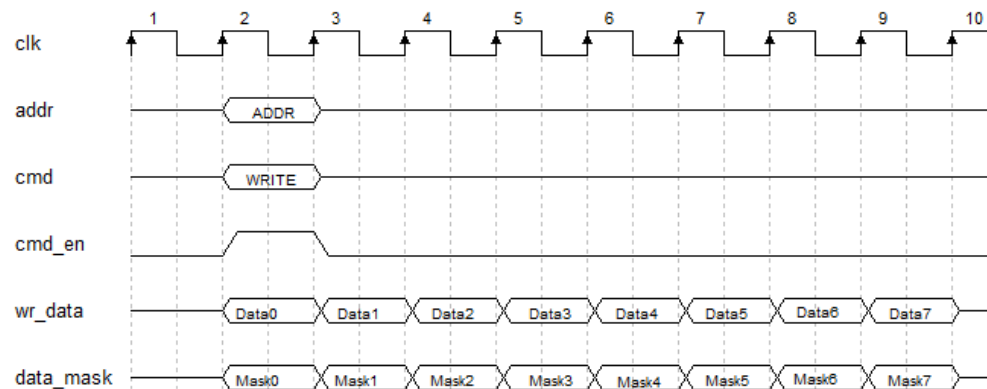
- There are multiple timing situations between the data channel and the command channel. Take the 16 burst length as an example.
- The write operation mode of two-channel PSRAM IP and single-channel PSRAM IP is the same, but the command and address of the two-channel PSRAM IP are independent, and write data need to be provided respectively.

Figure 4-8 Write Data Port Timing



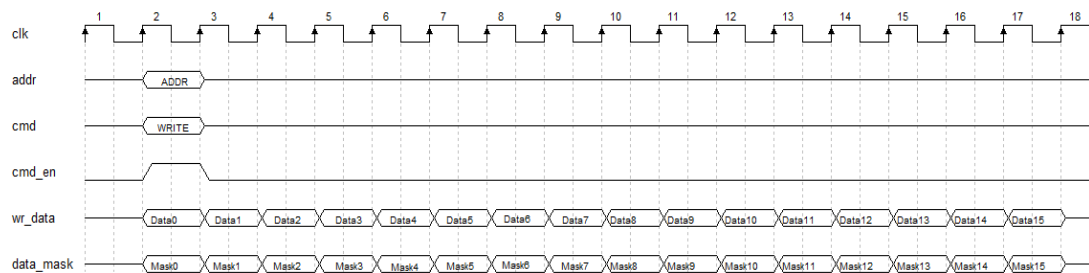
- The write data occupies 8 CLK cycles if the burst length is 32, as shown in Figure 4-9.
- If the mask function is not used, the data_mask can be 0.

Figure 4-9 Write Data Timing with Burst Length of 32



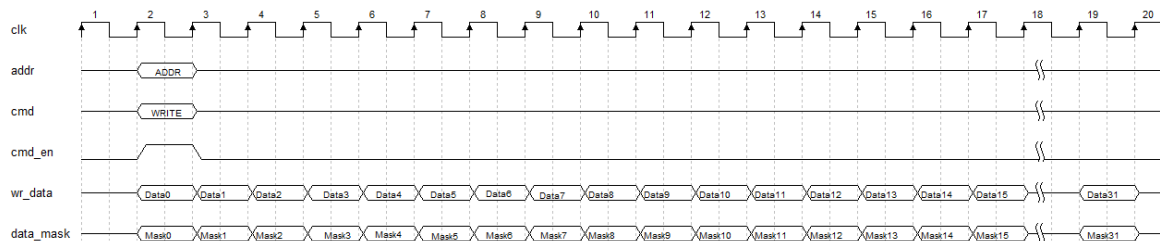
- The write data occupies 16 CLK cycles if the burst length is 64, as shown in Figure 4-10.
- If the mask function is not used, the data_mask can be 0.

Figure 4-10 Write Data Timing with Burst Length of 64



- The write data occupies 32 CLK cycles if the burst length is 128, as shown in Figure 4-11.
- If the mask function is not used, the data_mask can be 0.

Figure 4-11 Write Data Timing with Burst Length of 128



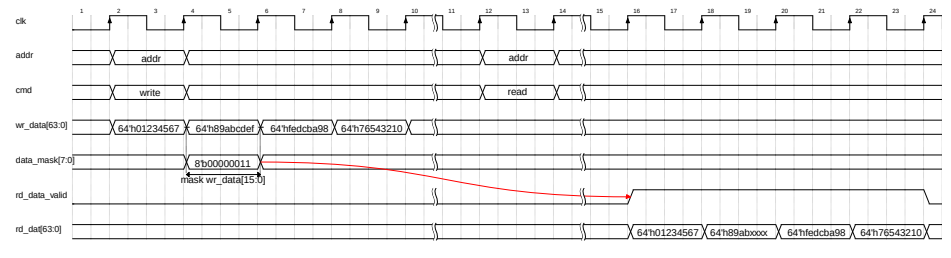
Data Mask (data_mask)

For data that the user does not need, the data mask signal (data_mask) can be used to mask the data. Each bit in data_mask controls one byte of wr_data, active high. The relationship is as follows: data_mask[0] controls wr_data[7:0], data_mask[1] controls wr_data[15:8], data_mask[2] controls

wr_data[23:16], and so on.

As shown in Figure 4-12, during the write operation, wr_data[15:0] = 16'hcdef is masked. Therefore, the current frame value 16'hcdef is not returned during the read operation. This is because when 16'hcdef is written to the PSRAM, it does not overwrite the original data at the corresponding PSRAM location. The value 16'hxxxx represents the data before write masking is applied.

Figure 4-12 data_mask and Read/Write Data Timing Diagram

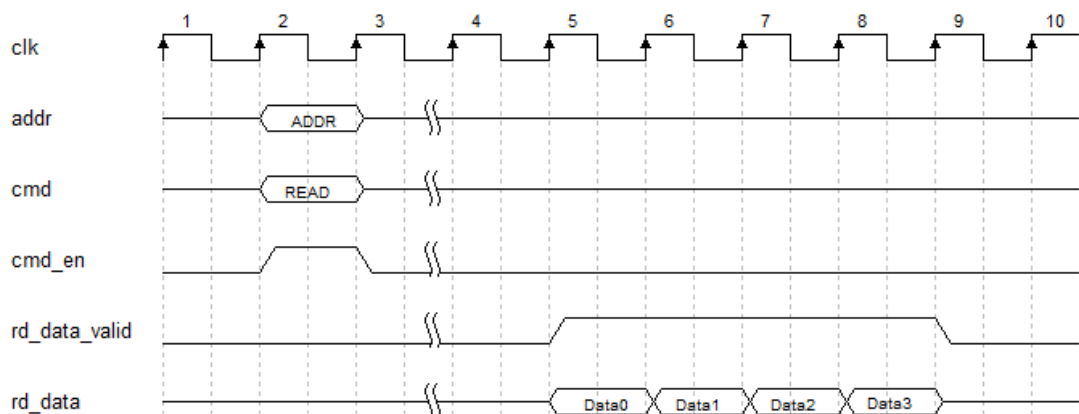


4.4.4 Read Data

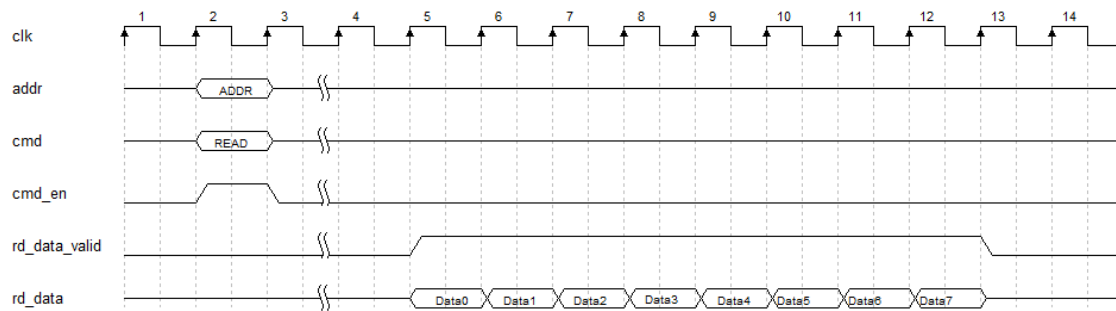
You can read the data from the PSRAM using the user ports rd_data and rd_data_valid.

- The rd_data port is the port for returned read data.
- The rd_data_valid signal indicates the validity of the read data. When it is high, the returned rd_data is valid at this time.
- There are multiple timing cases between the read data channel and the command channel. Take the 16 burst length as an example.
- The read operation mode of two-channel PSRAM IP and single-channel PSRAM IP is the same, but the command and address of the two-channel PSRAM IP are independent, and the rd_data_valid signal and rd_data data need to be received respectively.

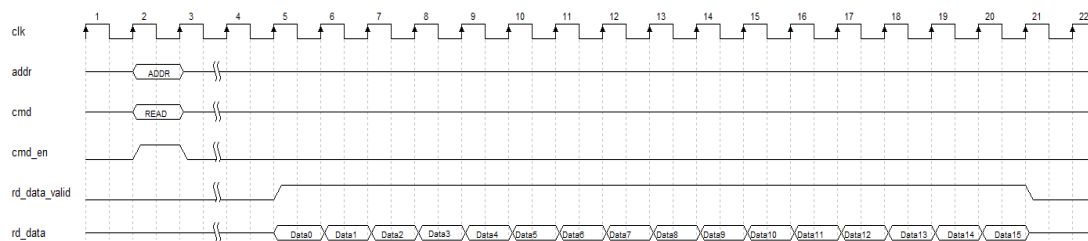
Figure 4-13 Read Data Port Timing



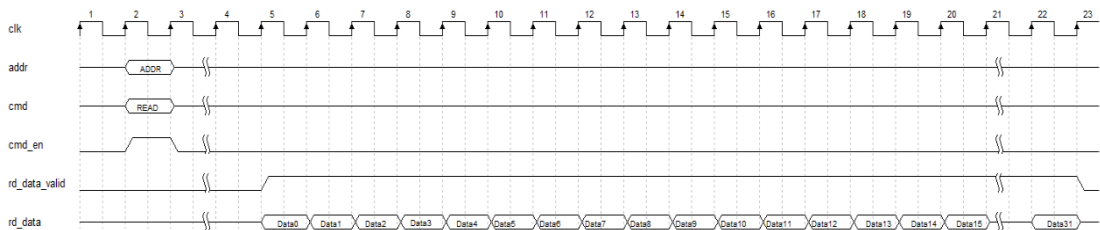
- The read data occupies 8 CLK cycles if the burst length is 32, as shown in Figure 4-14.

Figure 4-14 Read Data Timing with Burst Length of 32

- The read data occupies 16 CLK cycles if the burst length is 64, as shown in Figure 4-15.

Figure 4-15 Read Data Timing with Burst Length of 64

- The read data occupies 32 CLK cycles if the burst length is 128, as shown in Figure 4-16.

Figure 4-16 Read Data Timing with Burst Length of 128

5 Port List

When single-channel mode is selected, the I/Os of Gowin PSRAM Memory Interface HS IP are shown in Table 5-1.

Table 5-1 I/O List of Gowin PSRAM Memory Interface HS IP

Signal	Data Width	I/O	Description
User Interface			
addr	ADDR_WIDTH	Input	Address input
cmd	1	Input	Command channel
cmd_en	1	Input	Command and address enable signals 0: invalid 1: valid
cmd_rdy	1	Output	The assertion of cmd_en requires two conditions to be satisfied: • The Tcmd interval specified in Table 4-2 • cmd_rdy at logic 1
rd_data	4*DQ_WIDTH	Output	Read data channel
rd_data_valid	1	Output	rd_data valid signal 0: invalid 1: valid
wr_data	4*DQ_WIDTH	Input	Write data channel
data_mask	MASK_WIDTH	Input	Provides mask signal for wr_data
clk	1	Input	Reference input clock, it is usually on-board crystal oscillator clock
init_calib	1	Output	Initialization completed signal
clk_out	1	Output	The user- Logic design clock, with a frequency of 1/2 Memory Clk
rst_n	1	Input	Input reset signal 0: valid 1: invalid

Signal	Data Width	I/O	Description
memory_clk	1	Input	You can input chip working clock, which is generally a high clock of PLL frequency multiplication, or not use PLL.
pll_lock	1	Input	If memory_clk is PLL frequency doubling input, this interface is connected to PLL's pll_lock pin. If you do not use PLL, this interface is connected to 1'b1.
PSRAM Interface			
O_psram_cs_n	CS_WIDTH	Output	Chip selected, active-low.
O_psram_ck	CS_WIDTH	Output	A clock signal provided for PSRAM
O_psram_ck_n	CS_WIDTH	Output	Composes the differential signal with the O_psram_ck
O_psram_reset_n	CS_WIDTH	Output	PSRAM reset signal
IO_psram_dq	DQ_WIDTH	Bidirection	PSRAM data
IO_psram_rwds	RWDS_WIDTH	Bidirection	PSRAM data strobe signal and mask signal

When dual-channel mode is selected, the I/Os of Gowin PSRAM Memory Interface HS IP are shown in Table 5-2.

Table 5-2 I/O List of Gowin PSRAM Memory Interface HS IP

Signal	Data Width	I/O	Description
User Interface			
addr0	ADDR_WIDTH	Input	Channel 0 address input
addr1	ADDR_WIDTH	Input	Channel 1 address input
cmd_rdy0	1	Output	The assertion of cmd_en0 requires two conditions to be satisfied: ● The Tcmd interval specified in Table 4-2 ● cmd_rdy0 at logic 1
cmd_rdy1	1	Output	The assertion of cmd_en1 requires two conditions to be satisfied: ● The Tcmd interval specified in Table 4-2 ● cmd_rdy1 at logic 1
cmd0	1	Input	Channel 0 command channel
cmd1	1	Input	Channel 1 command channel
cmd_en0	1	Input	Channel 0 command and address enable signal 0: invalid

Signal	Data Width	I/O	Description
			1: valid
cmd_en1	1	Input	Channel 1 command and address enable signal 0: invalid 1: valid
rd_data0	[31:0]	Output	Read data channel 0
rd_data1	[31:0]	Output	Read data channel 1
rd_data_valid0	1	Output	Channel 0rd_data valid signal: 0: invalid 1: valid
rd_data_valid1	1	Output	Channel 1rd_data valid signal 0: invalid 1: valid
wr_data0	[31:0]	Input	Read data channel 0
wr_data1	[31:0]	Input	Read data channel 1
data_mask0	[3:0]	Input	Provides mask signal for channel 0wr_data
data_mask1	[3:0]	Input	Provides the mask signal for channel 1wr_data
init_calib0	1	Output	Channel 0 initialization completed signal
init_calib1	1	Output	Channel 1 initialization completed signal
clk	1	Input	Reference input clock, it is usually on-board crystal oscillator clock.
memory_clk	1	Input	You can input chip working clock, which is generally a high clock of PLL frequency multiplication, or not use PLL.
pll_lock	1	Input	If memory_clk is PLL frequency multiplication input, this interface is connected to PLL's pll_lock pin. If you do not use PLL, this interface is connected to 1'b1.
clk_out	1	Output	The user- logic design clock, with a frequency of 1/2 Memory Clk.
rst_n	1	Input	User input reset signal 0: valid 1: invalid
PSRAM Interface			
O_psram_cs_n	[1:0]	Output	Chip selected, active-low.
O_psram_ck	[1:0]	Output	A clock signal provided for PSRAM
O_psram_ck_n	[1:0]	Output	Composes the differential

Signal	Data Width	I/O	Description
			signal with the O_psram_ck
O_psram_reset_n	[1:0]	Output	PSRAM reset signal
IO_psram_dq	[15:0]	Bidirection	PSRAM data
IO_psram_rwds	[1:0]	Bidirection	PSRAM data strobe signal and mask signal

6 Parameters

Gowin PSRAM Memory Interface HS IP supports PSRAM devices. You need to configure each static parameter and timing parameter according to the design requirements, as shown in Table 6-1.

Table 6-1 Gowin PSRAM Memory Interface HS IP Static Parameters

Name	Description	Option
Memory TYPE	PSRAM type	W955D8MBYA, Custom.
CLK Ratio	Clock ratio of PSRAM PHY and internal logic, fixed.	1:2
Memory Clock	Expected frequency	50 MHz~166 MHz
Channel Number	Channel Selection	1 channel: Single-channel 2 channel: Dual-channel
Psram Width	PSRAM DQ width	8
Dq Width	Data width	8/16/24/32/40/48/56/64
Addr Width	Address width, you can write according to memory.	21
Data Width	User data width	4*Dq Width
CS Width	Chip selected width	Dq Width/Psram Width
Mask Width	Mask width	Data Width/Psram Width
Burst Mode	Data burst length	16/32/ 64/128
Burst Num	Number of data burst	Burst Mode/4
Fixed Latency Enable	Fixed latency enable	Fixed
Initial Latency	Initial latency	6
Drive Strength	Drive strength	35/50/100/200
Deep Power Down	Power option	"OFF", "ON"
Hybrid Sleep Mode	Sleep mode	"OFF", "ON"
Refresh Rate	Refresh rate	"normal", "faster"
PASR	Self refresh area	Full, bottom_1/2, bottom_1/4, bottom_1/8, top_1/2, top_1/4, top_1/8.

Name	Description	Option
Shift Delay	Shift delay	You can use the default value generally; if there is bit error with the temperature test, it can be adjusted appropriately with the range of 0 ~ 255.

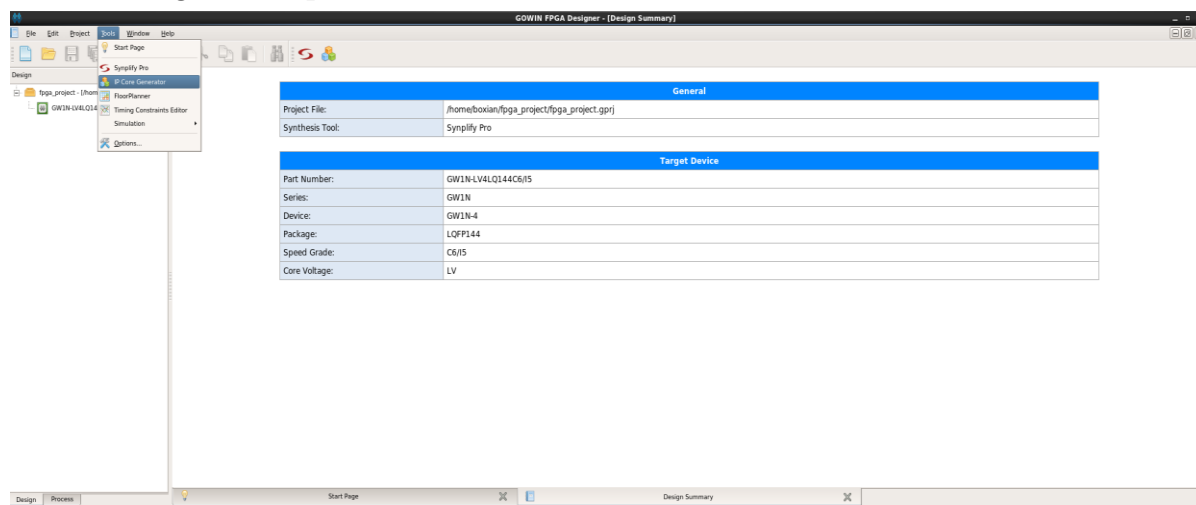
7 GUI

You can call and configure the Gowin PSRAM Memory Interface HS IP using the IP Core Generator in the IDE. In this chapter, take the "W955D8MBYA" PSRAM memory as an example, introduce the main configuration interface and options.

1. Open IP Core Generator.

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, as shown in Figure 7-1.

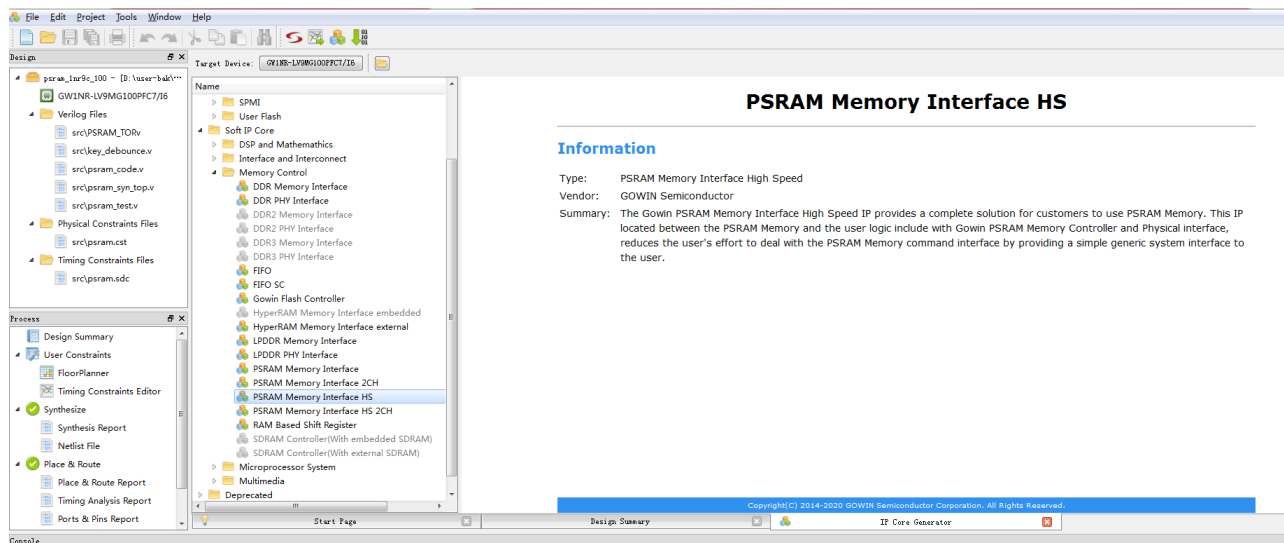
Figure 7-1 Open IP Core Generator



2. Open PSRAM Memory Interface HS IP core.

Click the "Memory Control", double-click "PSRAM Memory Interface HS", as shown in Figure 7-2.

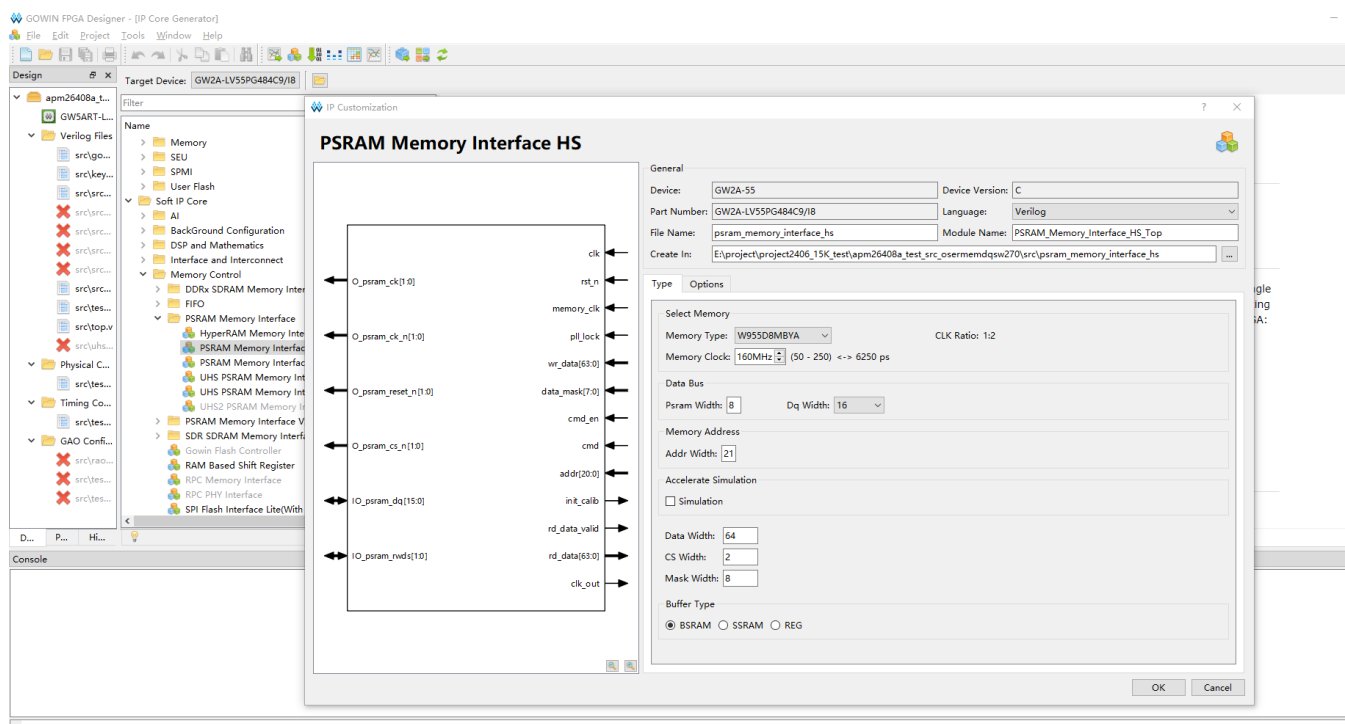
Figure 7-2 Open PSRAM Interface HS IP core



3. PSRAM Memory Interface HS IP Core Interface.

The left side of the configuration interface shows the PSRAM Memory Interface HS IP port diagram, as illustrated in Figure 7-3. In the port diagram, the right side represents the interface between the PSRAM Memory Controller and the user logic. Users can connect their own design to the PSRAM Memory Interface HS IP to send and receive commands and data. The left side represents the interface between the PHY and the memory devices. By connecting the PSRAM Memory Interface HS IP to the required memory devices, users can perform data read and write operations. Depending on the configuration settings, the signal widths and the number of signals in the port diagram will vary accordingly.

Figure 7-3 IP Core Interface

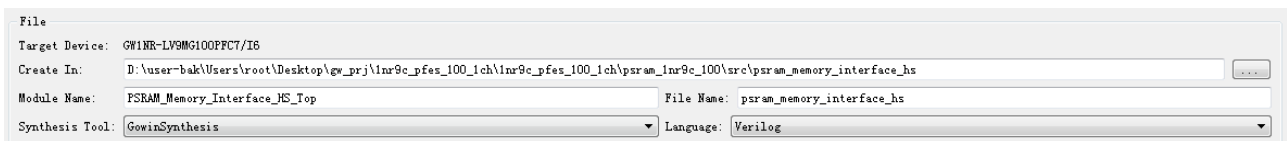


4. Configure General Information.

See the project general information in the configuration interface. Take GW1NR-9 chip as an example, and select the "MBGA100PF" package.

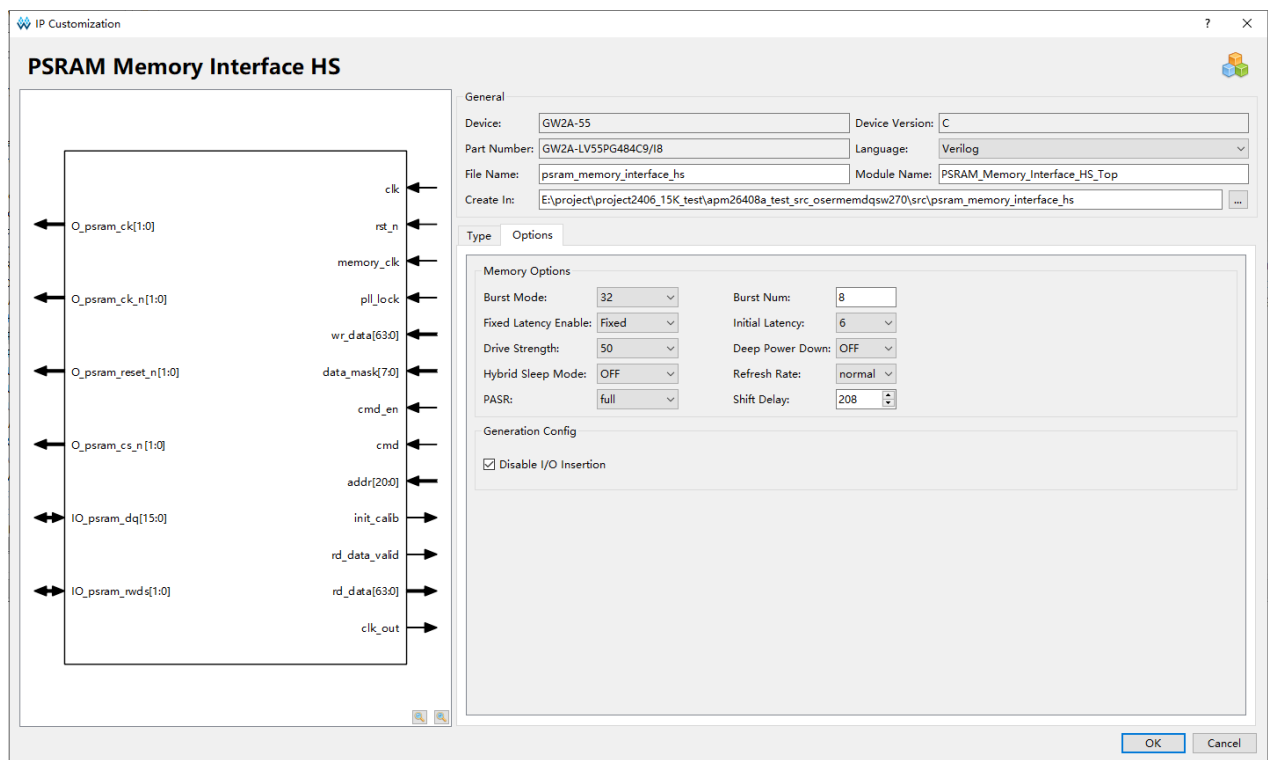
- The "Module Name" option displays the top-level file name of the generated project; the default value is "PSRAM_Memory_Interface_Top", and it can be modified.
- The "File Name" option displays the folder where the files are required by PSRAM Memory Interface HS IP core; the default value is "psram_memory_interface_hs", and it can be modified.
- "Create In" option displays the path the directory path where the IP folder will be generated, and it can be modified.

Figure 7-4 General Information Configuration Interface



5. For the parameter descriptions, you can see Chapter 6 *Parameters*.

Figure 7-5 Parameter Configuration



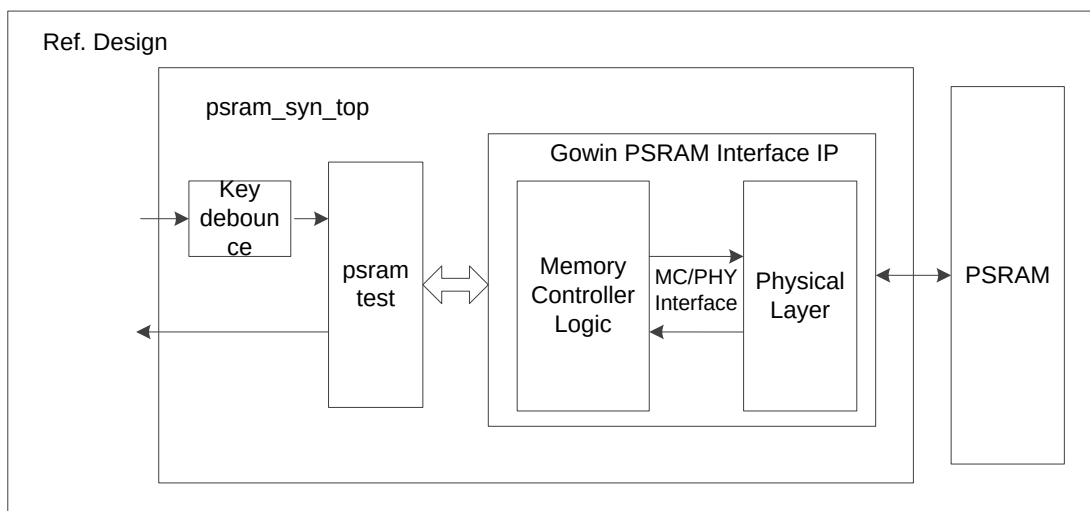
Note !

PSRAM HS 2CH IP: "Dq Width" and "Psram Width" parameters cannot be modified. The width of device with two PSRAMs has been configured according to the width of device with one PSRAM. The top-level file will be instantiated to two channels to generate a two-channel transmission, one PSRAM per channel. The width of device with four PSRAMs has been configured according to the width of device with two PSRAMs. The top-level file will be instantiated to two channels to generate a two-channel transmission, two PSRAMs per channel.

8 Reference Design

To quickly be familiar with and use Gowin PSRAM Memory Interface HS IP, a simple [reference design](#) is provided for you. The basic structure of reference is shown in Figure 8-1.

Figure 8-1 Block Diagram of Reference Design



In the reference design, the `psram_syn_top` module is the top-level module, and its ports are connected to the input reference clocks, external reset signals, etc., as shown in Table 8-1. The `psram_test` is used to generate the address, data, and read/write commands required by the Gowin PSRAM Interface HS IP, and the module can be synthesized. The `Key_debounce` module is a jitter elimination module that is used to eliminate the signal jitter generated by the key or dip switch when it controls the external stimulus.

Table 8-1 `psram_syn_top` Module Input Port List

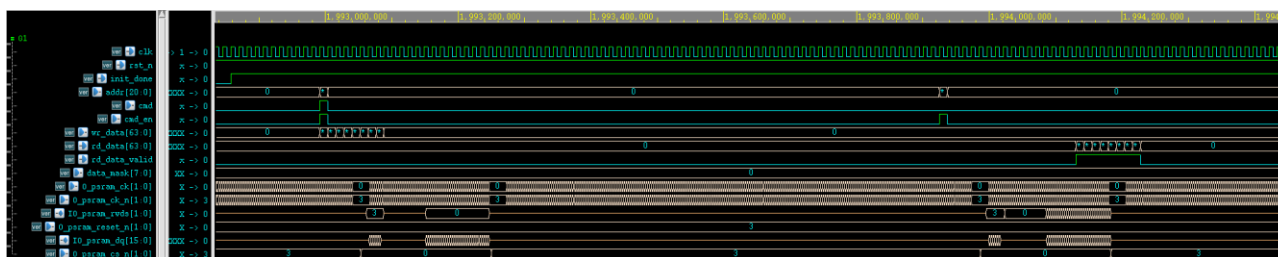
Name	Description
clk	Input reference clock, 50 MHz by default
rst_n	Input reset signal
init_calib	IP initialization success signal; high indicates the initialization is successful.
ERROR	Data check bit signal, high indicates that a data error is

Name	Description
	detected during read verification.

The `psram_test` module generates `n` consecutive write signals and data, and then performs `n` consecutive read operations on the written data for verification. After the verification is completed, the write-read operations are repeated in a loop. In this reference design, the memory device selected is W955D8MBYA, with Burst Mode configured to 128 and a DQ width of 16 bits.

The simulation waveforms of some signals between the `psram_test` and the PSRAM Memory Interface HS IP ports are shown in Figure 8-2 .

Figure 8-2 psram_test Port Signal Simulation Waveform



9 File Delivery

The delivery files for the Gowin PSRAM Memory Interface HS IP include the documents, the design source code, and the reference design.

9.1 Documents

The document folder mainly contains PDF file of the user guide.

Table 9-1 Document List

Name	Description
IPUG943, Gowin PSRAM Memory Interface HS IP User Guide	Gowin PSRAM Memory Interface HS IP User Guide

9.2 Design Source Code (Encryption)

The Encryption Code Folder contains the RTL encryption code of Gowin PSRAM Memory Interface HS IP used for the GUI, to generate the IP core as needed.

Table 9-2 Design Source Code List

Name	Description
PSRAM_TOP.v	The top-level file of the IP core, which provides you with interface information, unencrypted.
Gowin PSRAM Memory HS Interface partial code	
psram_code.v	Gowin PSRAM Memory Interface HS IP RTL source file, encrypted
psram_define.v	Gowin psram memory controller parameter definition module, which is generated by the user via the GUI, unencrypted.
psram_local_define.v	Gowin PSRAM memory controller parameter definition processing module, encrypted.
psram_param.v	Gowin PSRAM memory controller parameter configuration module, which is generated by the user via the GUI, unencrypted.
psram_local_param.v	Gowin PSRAM memory controller parameter processing module, which processes the parameters passed from the GUI, encrypted.

9.3 Reference Design

The Ref. Design folder contains the netlist file for Gowin PSRAM Memory Interface HS IP, the user reference design, the constraint file, the jitter elimination module, the top file, the project file folder, etc.

Table 9-3 Ref. Design Folder Contents List

Name	Description
psram_syn_top.v	The top module of reference design
key_debounce.v	Key jitter elimination module
psram_test.v	Test stimulus generation module
PSRAM_Memory_Interface_HS.vo	Gowin PSRAM Memory Interface HS IP netlist file
psram.cst	PSRAM physical constraints file
psram.sdc	PSRAM timing constraint file
psram.gao	Capture PSRAM chip data
PSRAM_Memory_Interface_HS	PSRAM HS IP project folder

