



Gowin Flash Controller IP

User Guide

IPUG901-1.8.5E, 06/13/2025

Copyright © 2025 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN is a trademark of Guangdong Gowin Semiconductor Corporation and are registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. All information in this document should be treated as preliminary. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
08/30/2019	1.0E	Initial version published.
10/24/2019	1.1E	● FLASH64KZ Register interface controller supported. ● FLASH608K Register interface controller supported. ● FLASH608K Wishbone interface controller supported.
11/04/2019	1.2E	FLASH256K Register interface and Wishbone interface controller of GW1NRF-4B devices supported.
11/18/2019	1.3E	● The user port design of FLASH96K controller simplified. ● The known simulation issues of FLASH96K controller fixed.
12/25/2019	1.4E	● FLASH64K Register interface controller supported. ● FLASH256K and FLASH608K AHB interface controller supported.
11/09/2020	1.5E	● FLASH128K Register interface controller supported. ● FLASH256K and FLASH608K AHB interface controller supported. ● FLASH256KA Register interface controller supported. ● FLASH256KA Wishbone interface controller supported. ● FLASH256KA AHB interface controller supported. ● FLASH256KA APB interface controller supported.
11/18/2021	1.6E	● FLASH96KA Register interface controller supported. ● FLASH96KA Wishbone interface controller supported. ● FLASH96KA AHB interface controller supported. ● FLASH96KA APB interface controller supported.
03/01/2022	1.7E	Controllers of FLASH96KA Wishbone, AHB and APB interfaces removed.
10/28/2022	1.8E	● FLASH256KA Register, AHB, APB, and Wishbone interface controller removed. ● FLASH128K Register interface controller removed.
11/24/2022	1.8.1E	A note of FLASH96KA added in section 3.1.1 Register Interface.
01/05/2023	1.8.2E	A note added in chapter 4 Signal Description.
01/13/2023	1.8.3E	The note in chapter 4 Signal Description updated.
02/03/2023	1.8.4E	The description of chapter 4 Signal Description updated.
06/13/2025	1.8.5E	The note in chapter 4 Signal Description updated.

Contents

Contents	i
List of Figures	ii
List of Tables	iii
1 About This Guide	1
1.1 Purpose	1
1.2 Related Documents	1
1.3 Terminology and Abbreviations	1
1.4 Support and Feedback	2
2 Function	3
2.1 Overview	3
2.2 Features	3
3 Operating Principle	4
3.1 Interface Operating Principle	4
3.1.1 Register Interface	4
3.1.2 Wishbone Interface	5
3.1.3 AHB Interface	5
3.1.4 APB Interface	5
3.2 Register Operating Principle	6
3.2.1 Row Address Register	6
3.2.2 Column Address Register	7
3.2.3 Read Data Register	7
3.2.4 Write Data Register	7
3.2.5 Command Register	7
3.2.6 Status Register	7
3.2.7 Start Flag Register	7
4 Signal Description	8
5 Parameter Definition	10
6 Interface Configuration	12
7 Reference Design	13

List of Figures

Figure 3-1 Register Interface	4
Figure 3-2 Wishbone Interface.....	5
Figure 3-3 AHB Interface	5
Figure 3-4 APB Interface.....	6
Figure 6-1 Gowin Flash Controller IP GUI	12

List of Tables

Table 1-1 Terminology and Abbreviations	1
Table 3-1 Flash Controller Register List.....	6
Table 4-1 Signal Definition of Gowin Flash Controller	8
Table 5-1 Parameter Definition of Gowin Flash Controller	11

1 About This Guide

1.1 Purpose

The purpose of Gowin Flash Controller IP User Guide is to help you learn the features and usage of Gowin Flash Controller IP by providing the descriptions of the functions, signal definition, working principle, and GUI.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS891, GW1NRF series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)
- [UG295, Gowin User Flash User Guide](#)

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
AHB	Advanced High Performace Bus
APB	Advanced Peripheral Bus
FPGA	Field Programmable Gate Array
MCU	Microcontroller Unit
IP	Intellectual Property

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Function

2.1 Overview

Gowin Flash Controller includes four interfaces: Register interface, AHB interface, APB interface, and Wishbone bus interface. Through AHB interface, APB interface, and Wishbone bus interface, it can connect and communicate with MCU.

2.2 Features

Gowin Flash Controller IP features include:

- Supports the read and write operations of FLASH96K Register interface.
- Supports the read and write operations of FLASH256K Register interface, AHB interface, APB interface, and Wishbone bus interface.
- Supports the read and write operations of FLASH96KA Register interface.
- Supports the read and write operations of FLASH608K Register interface, AHB interface, APB interface, and Wishbone bus interface.
- Supports the read and write operations of FLASH64KZ Register interface.
- Supports the read and write operations of FLASH64K Register interface.
- Through AHB interface, APB interface, and Wishbone bus interface, it can connect and communicate with MCU.

3 Operating Principle

3.1 Interface Operating Principle

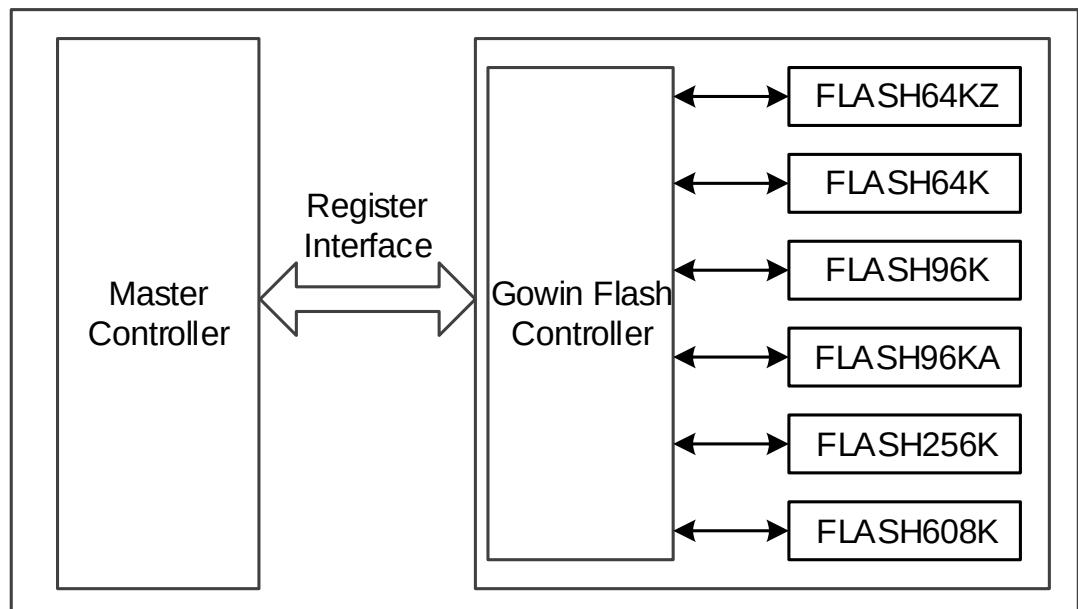
3.1.1 Register Interface

Through the Register interface, the master controller transfers instruction or data to Gowin Flash Controller IP which then sends them to FLASH96K, FLASH96KA, FLASH256K, FLASH64KZ, FLASH64K, or FLASH608K; or the data of FLASH96K, FLASH96KA^[1], FLASH256K, FLASH64KZ, FLASH64K, and FLASH608K are transmitted to the master controller through Gowin Flash Controller IP Register interface, as shown in Figure 3-1.

Note!

- [1] Read: 12 clks
- [1] Pulse width of Done signal is 2 clks.

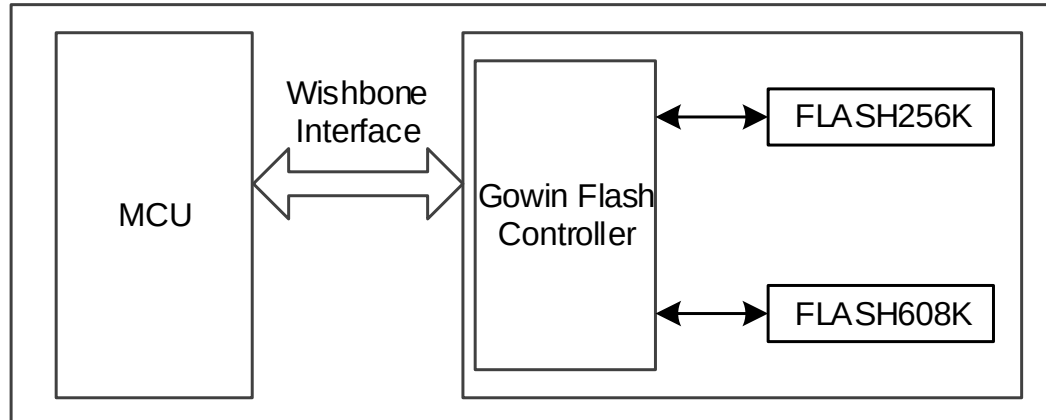
Figure 3-1 Register Interface



3.1.2 Wishbone Interface

Through Wishbone bus interface, MCU transfers instruction or data to Gowin Flash Controller IP which then sends them to FLASH608K or FLASH256K; or the data of FLASH608K and FLASH256K are transmitted to MCU through Gowin Flash Controller IP Wishbone bus interface, as shown in Figure 3-2.

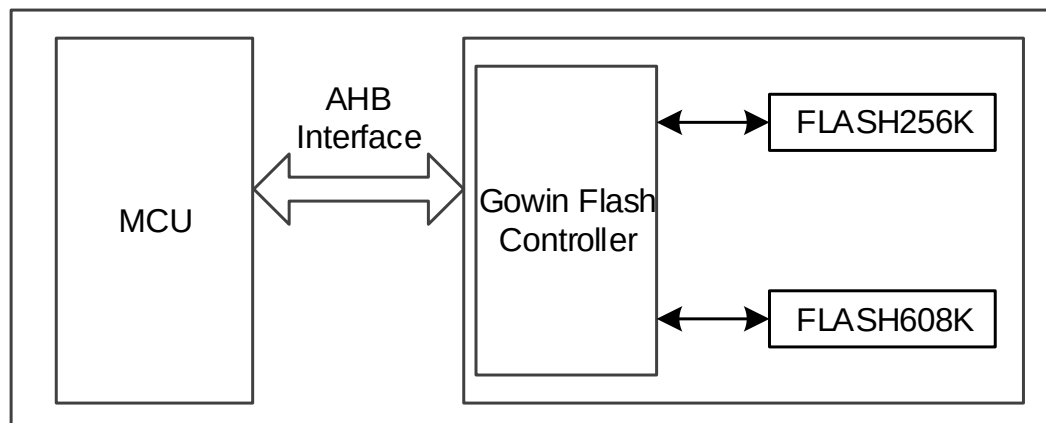
Figure 3-2 Wishbone Interface



3.1.3 AHB Interface

Through AHB interface, MCU transfers instruction or data to Gowin Flash Controller IP which then sends them to FLASH608K or FLASH256K.; or the data of FLASH608K and FLASH256K are transmitted to MCU through Gowin Flash Controller IP AHB interface, as shown in Figure 3-3.

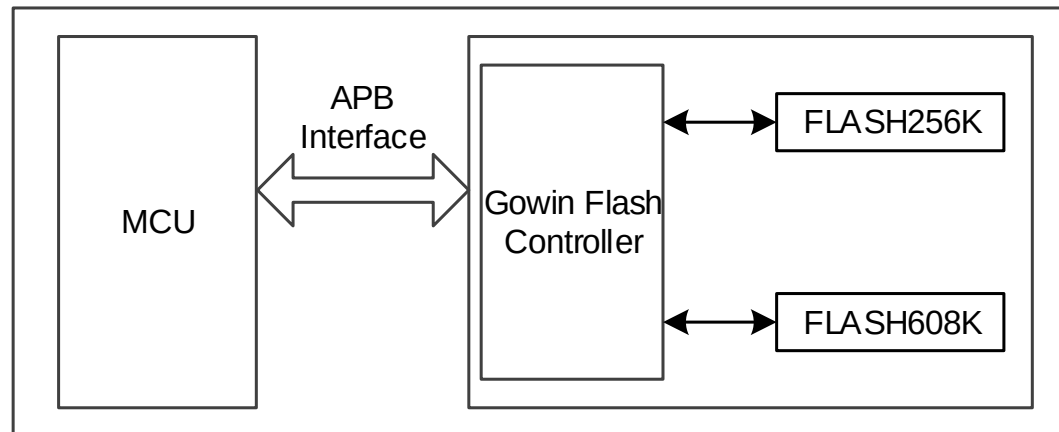
Figure 3-3 AHB Interface



3.1.4 APB Interface

Through APB interface, MCU transfers instruction or data to Gowin Flash Controller IP which then sends them to FLASH608K or FLASH256K; or the data of FLASH608K or FLASH256K are transmitted to MCU through Gowin Flash Controller IP APB interface, as shown in Figure 3-4.

Figure 3-4 APB Interface



3.2 Register Operating Principle

Gowin Flash Controller IP with Wishbone interface, AHB interface, or APB interface has the same registers as follows.

- Line Address Register
- Column Address Register
- Read Data Register
- Write Data Register
- Command register
- Status Register
- Start Flag Register

Table 3-1 Flash Controller Register List

Name	Address	Width	Type	Description
XADDR	0x00	9, 7, 6 or 5	Read/Write	Line Address Register
YADDR	0x04	6	Read/Write	Column Address Register
RDATA	0x08	32	Read-only	Read Data Register
WDATA	0x0C	32	Read/Write	Write Data Register
CR	0x10	8	Read/Write	Command Register
SR	0x14	8	Read-only	Status Register
START	0x18	1	Read/Write	Start Flag Register

The user reads and writes the above registers through the Wishbone, AHB or APB interface, thus realizing the read, write and erase operations on the Flash.

3.2.1 Row Address Register

The row address register address of Flash controller is 0x00, and this register stores the row address of the Flash. FLASH608K controller corresponds to 9-bit width; FLASH256K controller corresponds to 7-bit width; FLASH96K and FLASH96KA controllers correspond to 6-bit width, FLASH64KZ and FLASH64K controllers correspond to 5-bit width.

3.2.2 Column Address Register

The column address register address of Flash controller is 0x04 with a width of 6 bits, which stores the column address data of the Flash.

3.2.3 Read Data Register

The read data register address of Flash controller is 0x08 with a width of 32 bits, which stores data read from Flash.

3.2.4 Write Data Register

The write data register address of Flash controller is 0x0C with a width of 32 bits, which stores data to write in Flash.

3.2.5 Command Register

The instruction register address of Flash controller is 0x10 with a width of 8 bits, which only use two of the bits ([1: 0]). If CR[1:0] = 2'b10, then perform erase operation. If CR[1:0] = 2'b01, then perform write operation. If CR[1:0] = 2'b00, then perform read operation.

3.2.6 Status Register

The status register address of Flash controller is 0x14 with a width of 8 bits, which only use the lowest bit. It receives a finish signal from the Flash controller for a read, write, or erase operation. SR[0] = 1'b1 indicates the read, write, or erase operation has finished.

3.2.7 Start Flag Register

The Start Flag register address of Flash controller is 0x18 with a width of 1 bit. When the START value of Start Flag Register is 1 and the SR[0] value of Status Register is 0, the Flash controller starts to work.

4 Signal Description

The signal definition of Gowin Flash Controller is as shown in Table 4-1. The correspondences between User Flash primitives and devices supported are shown in Table 3-1 of [UG295, Gowin User Flash User Guide](#).

Table 4-1 Signal Definition of Gowin Flash Controller

No.	Signal Name	I/O	Width	Description	Note
1	clk_i	input	1	Clock signal	Primitive: FLASH96K Interface: Register
2	nrst_i	input	1	Reset signal	
3	r_en_i	input	1	Read enable signal	
4	clear_page_enable_i	input	1	Clear page enable signal	
5	prog_enable_i	input	1	Program enable signal	
6	write_page_enable_i	input	1	Write page enable signal	
7	erase_en_i	input	1	Erase enable signal	
8	pre_prog_i	input	1	Pre-program signal	
9	wyaddr_i	input	[8:0]	Write Y direction address	
10	wxaddr_i	input	[5:0]	Write X direction address	
11	page_address	input	[5:0]	Page address	
12	wdata_i	input	[31:0]	Write data into flash	
13	rdata_o	output	[31:0]	Read data from flash	
14	done_flag_o	output	1	Completely flag	
15	wb_clk_i	input	1	Master system clock	- Primitive: FLASH256K Interface: Wishbone Interface - Primitive: FLASH608K Interface: Wishbone
16	wb_rst_i	input	1	Synchronous active high reset	
17	wb_addr_i	input	[4:0]	Lower address bits	
18	wb_data_i	input	[31:0]	Data bus input	
19	wb_data_o	output	[31:0]	Data bus output	
20	wb_we_i	input	1	Write enable	
21	wb_stb_i	input	1	strobe/core select	
22	wb_cyc_i	input	1	Valid bus cycle	

No.	Signal Name	I/O	Width	Description	Note
23	wb_ack_o	output	1	Bus cycle acknowledge	● Primitive: FLASH96KA Interface: Register ● Primitive: FLASH256K Interface: Register ● Primitive: FLASH608K Interface: Register ● Primitive: FLASH64KZ, FLASH64K Interface: Register
24	wdata_i	input	[31:0]	Write data into flash	
25	wyaddr_i	input	[5:0]	Write Y direction address	
26	wxaddr_i	input	[8/6/5/4:0]	Write X direction address	
27	erase_en_i	input	1	Erase enable	
28	done_flag_o	output	1	Completely flag	
29	start_flag_i	input	1	Beginning flag	
30	clk_i	input	1	Clock signal	
31	nrst_i	input	1	Reset signal	
32	rdata_o	output	[31:0]	Read data from flash	
33	wr_en_i	input	1	Write or read enable 1 : Write enable 0 : Read enable	● Primitive: FLASH64K Interface: Register ● Primitive: FLASH96KA Interface: Register
34	sleep_i	input	1	Control sleep status dynamically	
35	AHB_HRDAT A	output	[31:0]	Read data bus	● Primitive: FLASH256K Interface: AHB ● Primitive: FLASH608K Interface: AHB
36	AHB_HREADY	output	1	Slave ready	
37	AHB_HRESP	output	[1:0]	Slave response	
38	AHB_HTRANS	input	[1:0]	Transfer type	
39	AHB_HSIZE	input	[2:0]	Transfer size	
40	AHB_HWRITE	input	1	Transfer direction	
41	AHB_HADDR	input	[31:0]	Address bus	
42	AHB_HWDAT A	input	[31:0]	Write data bus	
43	AHB_HSEL	input	1	Slave chip select	
44	AHB_HCLK	input	1	System clock	
45	AHB_HRESETn	input	1	System reset	● Primitive: FLASH256K Interface: APB ● Primitive: FLASH608K Interface: APB
46	PRDATA	output	[31:0]	Read data bus	
47	PREADY	output	1	Slave ready	
48	PCLK	input	1	System clock	
49	PSEL	input	1	Select signal	
50	PENABLE	input	1	Enable signal	
51	PWRITE	input	1	Write signal	

No.	Signal Name	I/O	Width	Description	Note
52	PADDR	input	[31:0]	Address signal	
53	PWDATA	input	[31:0]	Write Data	
54	PRESETn	input	1	System reset	

Note!

- clk_i requires a clock frequency of 50 MHz and a period of 20 ns. The value of Erase operation (page erase) counter in the code is 5501000. Therefore, the duration from the moment erase_en_i and start_flag_i are asserted to the moment done_flag_o goes high is $20 \text{ ns} \times 5,501,000 = 110.02 \text{ ms}$.
- The value of write operation (32-bit data) counter in the code is 2500. Therefore, the duration from the moment wr_en_i and start_flag_i are asserted to the moment done_flag_o goes high is $20 \text{ ns} \times 2500 = 50 \text{ us}$.
- The actual clk_i clock frequency can be lower than 50 MHz, but the operating time will be longer. For example, if the clk_i clock frequency is 25 MHz, and the period is 40 ns, the duration from the moment erase_en_i and start_flag_i are asserted to the moment done_flag_o goes high is $40 \text{ ns} \times 5501000 = 220.04 \text{ ms}$; the duration from the moment wr_en_i and start_flag_i are asserted to the moment done_flag_o goes high is $40 \text{ ns} \times 2500 = 100 \text{ us}$.
- The code may be updated; the above data are estimates based on a 50 MHz clock condition and are for reference only. For accurate timing, it is recommended to combine the Flash timing diagram with simulation results.

5 Parameter Definition

The parameter definition of Gowin Flash Controller IP is as shown in Table 5-1.

Table 5-1 Parameter Definition of Gowin Flash Controller

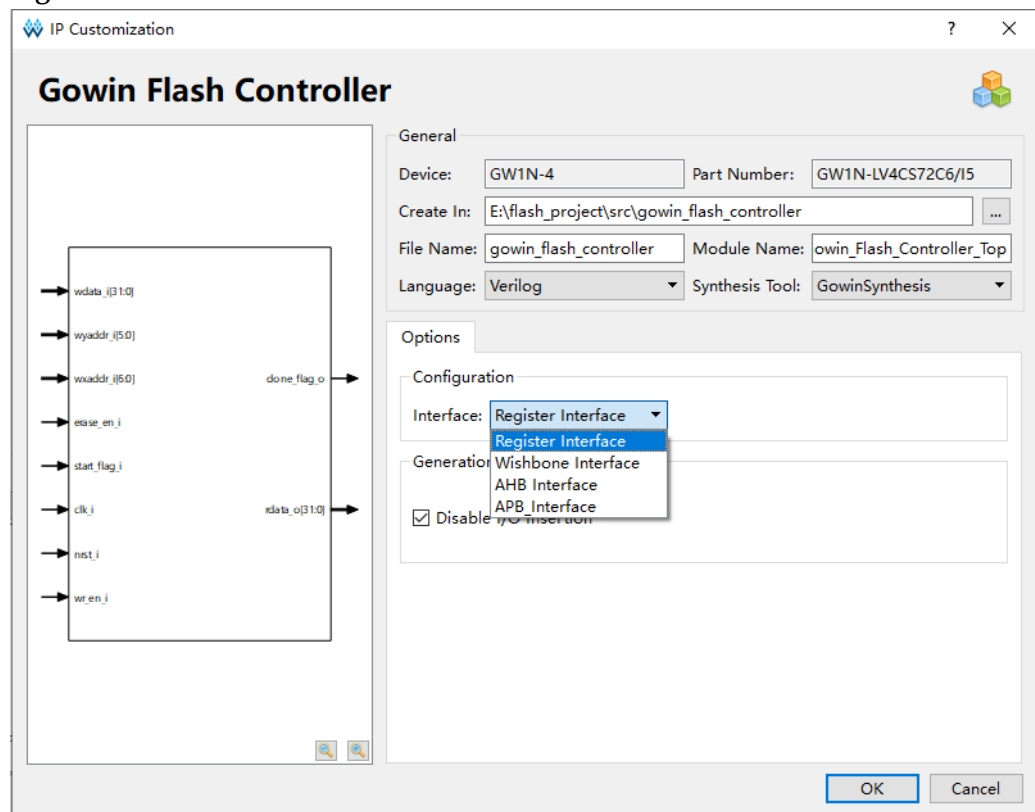
Name	Description	Value
Interface	Gowin Flash Controller Interface Configuration	● Register Interface ● AHB Interface ● APB Interface ● Wishbone Interface

6 Interface Configuration

You can call and configure Gowin Flash Controller IP using the IP core generator tool in the IDE.

Gowin Flash Controller IP GUI is as shown in Figure 6-1.

Figure 6-1 Gowin Flash Controller IP GUI



7 Reference Design

Please refer to the Gowin Flash Controller [Reference Design](#) for details at Gowinsemi website.

