



Gowin DDR Memory Interface IP

Release Note

RN507-1.0E,03/22/2018

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Revision History

Date	Version	Description
03/22/2018	1.0E	Initial version published.

Contents

Contents i

1 About This Release 1

2 Overview..... 2

3 File 3

4 IP Support..... 4

1 About This Release

This release includes Gowin DDR Memory Interface IP reference design and IP Core Generator supports Gowin I3C IP generation.

Gowin DDR Memory Interface IP reference design is available at Gowin Website. Take a specific parameter as an example for the reference design, which can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

2Overview

Gowin DDR Memory Interface IP is a common DDR memory interface IP that complies with the JESD79F standard protocol. Gowin DDR Memory Interface IP provides the user a generic command interface to connect with the memory chip to access and save. The IP includes the DDR Memory Controller (MC) and the corresponding Physical Interface (PHY) design.

Table 2-1 Gowin DDR Memory Interface IP

Gowin DDR Memory Interface IP	
IP Core Application	
Supported Devices	GW2A-18, GW2AR-18, GW2A-55
Delivered Files	
Design Files	Verilog (encrypted)
Reference Designs	Verilog
TestBench	Verilog
Test and Design Flow	
Integrated Software	Synplify Pro_N-2017.09G-SP1-Beta2
Application Software	GowinYunYuan_V1.8.0Beta1

3File

The software release file contains Gowin DDR Memory Interface IP User Guide, which is listed below:

File	IP Core Generation
Gowin DDR Memory Interface IP User Guide.pdf	PDF

4 IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not have associated FPGA specific location (.cst) and timing constraints (.sdc) documents, which the user can determine as required.

For the customized IP design and support, please contact Gowin sales and support line.

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