GW1NRF series of Bluetooth FPGA Products

Package & Pinout User Guide

UG893-1.0.2E, 08/08/2025

Copyright © 2025 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

GOWIN is the trademark of Guangdong Gowin Semiconductor Corporation and are registered in China, the U.S. Patent and Trademark Office, and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders. No part of this document may be reproduced or transmitted in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision History

Date	Version	Description
11/12/2019	1.0E	Initial version published.
12/15/2022	1.0.1E	● Package diagrams updated. ● The note of “Table 2-4 Definition of the Pins in the GW1NRF series of Bluetooth FPGA products” in “2.5 Pin Definitions” added.
08/08/2025	1.0.2E	● The description of “2.5 I/O BANK Introduction” optimized. ● Recommended PCB Layout diagrams added.

Contents

Contents i
List of Figures ii
List of Tables iii
1 About This Guide 1
1.1 Purpose 1
1.2 Related Documents 1
1.3 Terminology and Abbreviations 1
1.4 Support and Feedback 2
2 Overview 3
2.1 PB-Free Package 3
2.2 Package, Max. User I/O Information, and LVDS Paris 3
2.3 Power Pin 4
2.4 Pin Quantity 4
2.4.1 Quantity of GW1NRF-4B Pins 4
2.5 I/O BANK Introduction 5
3 View of Pin Distribution 6
3.1 View of GW1NRF-4B Pins Distribution 6
3.1.1 View of QN48 Pins Distribution 6
3.1.2 View of QN48E Pins Distribution 7
4 Package Diagrams 8
4.1 QN48 Package Outline (6mm x 6mm) 8
4.2 QN48E Package Outline (6mm x 6mm) 10

List of Figures

Figure 3-1 View of GW1NRF-4B QN48 Pins Distribution (Top View) 6
Figure 3-2 View of GW1NRF-4B QN48E Pins Distribution (Top View) 7
Figure 4-1 Package Outline QN48 8
Figure 4-2 Recommended PCB Layout QN48 9
Figure 4-3 Package Outline QN48E 10
Figure 4-4 Recommended PCB Layout QN48E 11

List of Tables

Table 1-1 Abbreviation and Terminology 1
Table 2-1 Package, Max. User I/O Information, and LVDS Paris 3
Table 2-2 Other Pins in the GW1NRF Series 4
Table 2-3 Quantity of GW1NRF-4B Pins 4
Table 3-1 Other pins in GW1NRF-4B QN48 7
Table 3-2 Other pins in GW1NRF-4B QN48E 7

1 About This Guide

1.1 Purpose

This manual contains an introduction to the GW1NRF series of Bluetooth FPGA products together with a definition of the pins, list of pin numbers, distribution of pins, and package diagrams.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- DS891, GW1NRF series of Bluetooth FPGA products Data Sheet
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG893, GW1NRF series of Bluetooth FPGA products Package and Pinout
- UG892, GW1NRF-4B Pinout

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviation and Terminology

Terminology and Abbreviations	Full Name
FPGA	Field Programmable Gate Array
SIP	System in Package
QN	QFN package

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

The GW1NRF series of FPGA products are the first generation products in the LittleBee® family and represent one form of SoC FPGA. The GW1NRF series of FPGA products integrate 32 bits hardcore processor and support Bluetooth 5.0 Low Energy radio. They have abundant logic units, IOs, built-in B-SRAM and DSP resources, power management module, and security module. The GW1NRF series provides low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage.

2.1 PB-Free Package

The GW1NRF series of Bluetooth FPGA products are PB free in line with the EU ROHS environmental directives. The substances used in the GW1NRF series of Bluetooth FPGA products are in full compliance with the IPC-1752 standards.

2.2 Package, Max. User I/O Information, and LVDS Paris

Table 2-1 Package, Max. User I/O Information, and LVDS Paris

Package	Pitch (mm)	Size (mm)	GW1NRF-4B
QN48	0.4	6 x 6	25(4)
QN48E	0.4	6 x 6	25(4)

Note!

- In this manual, abbreviations are employed to refer to the package types. See 1.3 Terminology and Abbreviations.
- See GW1NRF series of Bluetooth FPGA Products Data Sheet for more details.
- The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously.

2.3 Power Pin

Table 2-2 Other Pins in the GW1NRF Series

VCC	VCCIO0	VCCIO1	VCCIO2
VCCIO3	VCCX	VSS	

2.4 Pin Quantity

2.4.1 Quantity of GW1NRF-4B Pins

Table 2-3 Quantity of GW1NRF-4B Pins

Pin Type		GW1NRF-4B	
		QN48	QN48E
I/O Single end/Differential pair/LVDS[1]	BANK0	9/4/0	9/4/0
	BANK1	4/1/1	4/1/1
	BANK2	8/4/3	8/4/3
	BANK3	4/1/0	4/1/0
Max. User I/O[2]		25	25
Differential Pair		10	10
True LVDS output		4	4
VCC		2	2
VCCX		1	1
VCCIO0/VCCIO3[3]		1	1
VCCIO1/VCCIO2[3]		1	1
VSS		2	1
MODE0		0	0
MODE1		0	0
MODE2		0	0
JTAGSEL_N		1	1

Note!

- [1] The number of single end/ differential/LVDS I/O includes CLK pins and download pins.
- [2] The JTAGSEL_N and JTAG pins are exclusive. The JTAGSEL_N pin and the four pins of JTAG (TCK, TDI, TDO, and TMS) cannot be simultaneously used as I/O.
- [3] Pin multiplexing.

2.5 I/O BANK Introduction

There are four I/O Banks in the GW1NRF series of FPGA products.

Please refer to DS891, GW1NRF series of Bluetooth FPGA Products Data Sheet > 3.4 Input/Output Blocks for detailed Bank distribution schematic.

This manual provides an overview of the distribution view of the pins in the GW1NRF series of Bluetooth FPGA products. Please refer to 3 View of Pin Distribution for further details. The different I/O Banks that form the GW1NRF series of Bluetooth FPGA products are marked with different colors.

Various symbols are used for the user I/O, power, and ground. The various symbols and colors used for the various pins are defined as follows:

- " " denotes the I/O in BANK0.
- " " denotes the I/O in BANK1.
- " " denotes the I/O in BANK2.
- " " denotes the I/O in BANK3.
- " " denotes VCC, VCCX, and VCCIO.
- " " denotes VSS.
- " " denotes NC.
- “ ” denotes BLE.

3 View of Pin Distribution

3.1 View of GW1NRF-4B Pins Distribution

3.1.1 View of QN48 Pins Distribution

Figure 3-1 View of GW1NRF-4B QN48 Pins Distribution (Top View)

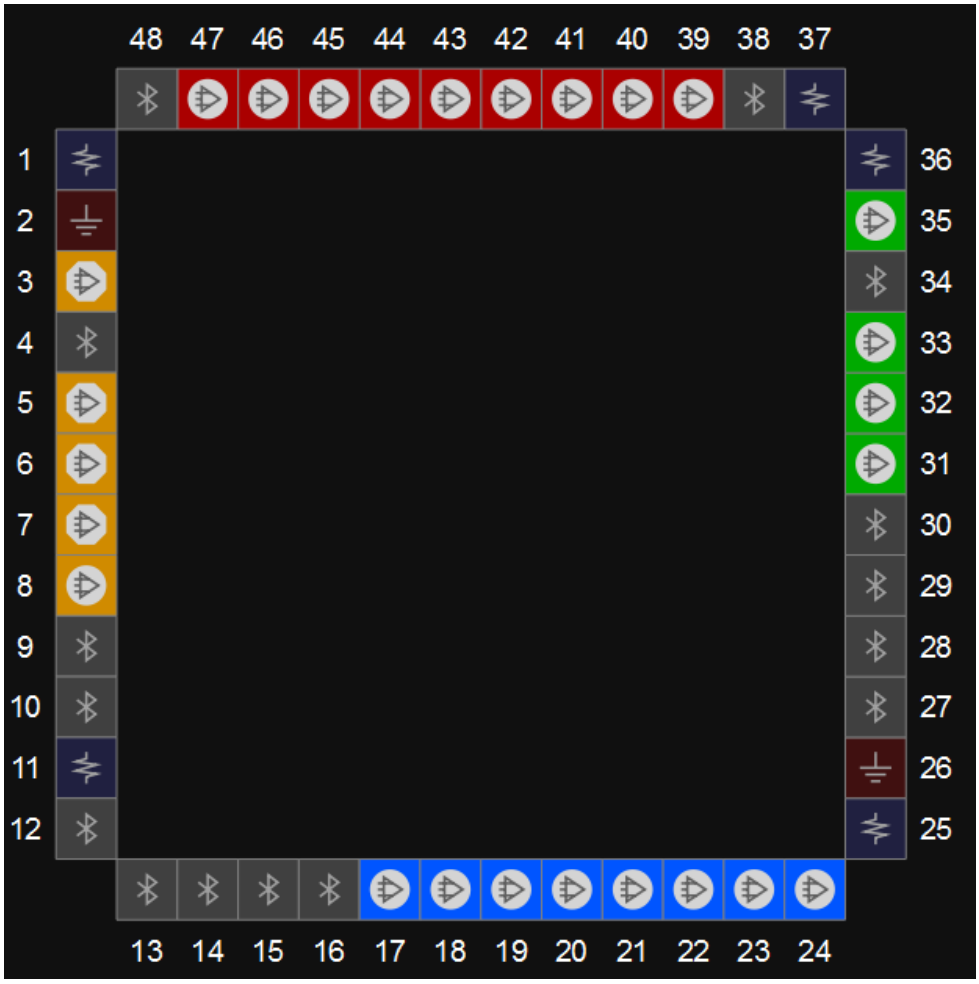


Table 3-1 Other pins in GW1NRF-4B QN48

VCC	11,37
VCCX	36
VCCIO0/VCCIO3	1
VCCIO1/VCCIO2	25
VSS	26,2

3.1.2 View of QN48E Pins Distribution

Figure 3-2 View of GW1NRF-4B QN48E Pins Distribution (Top View)

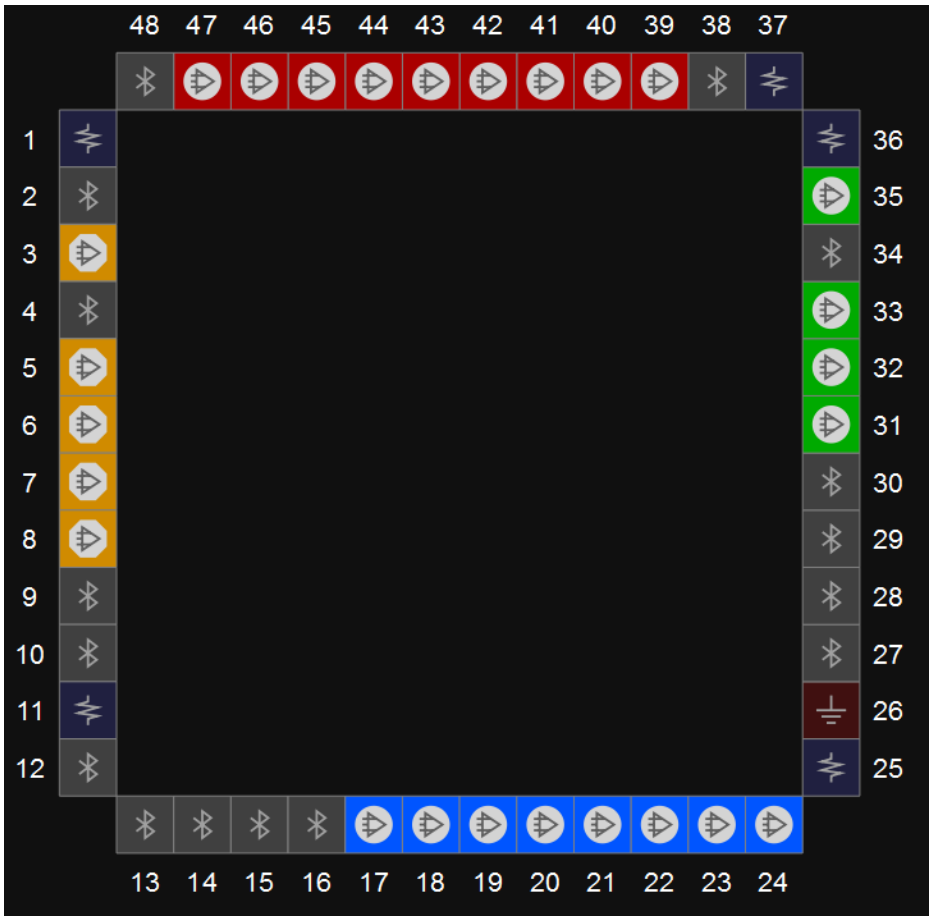


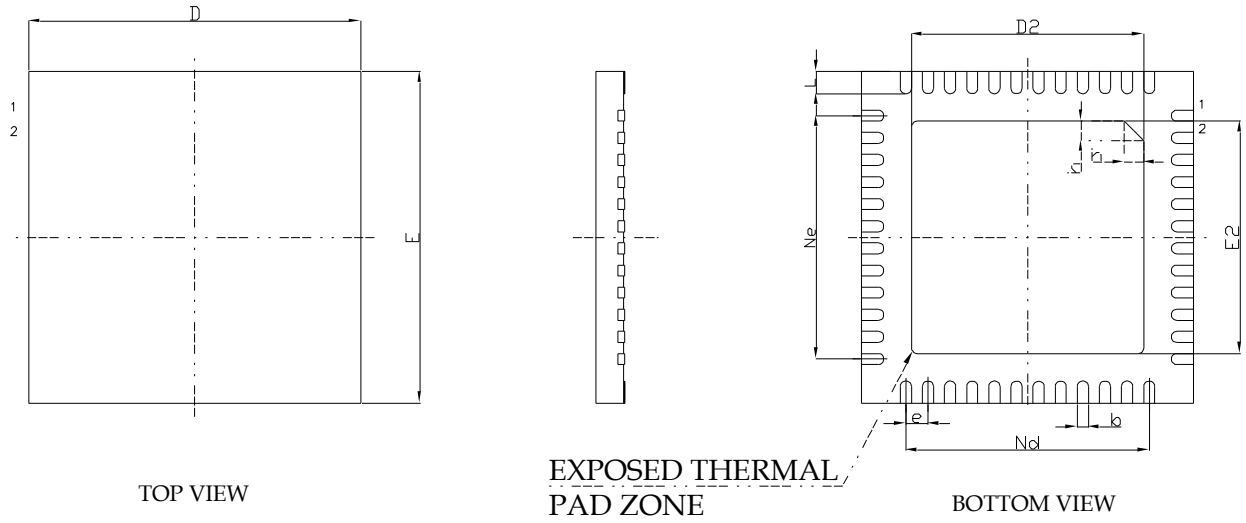
Table 3-2 Other pins in GW1NRF-4B QN48E

VCC	11,37
VCCX	36
VCCIO0/VCCIO3	1
VCCIO1/VCCIO2	25
VSS	26

4 Package Diagrams

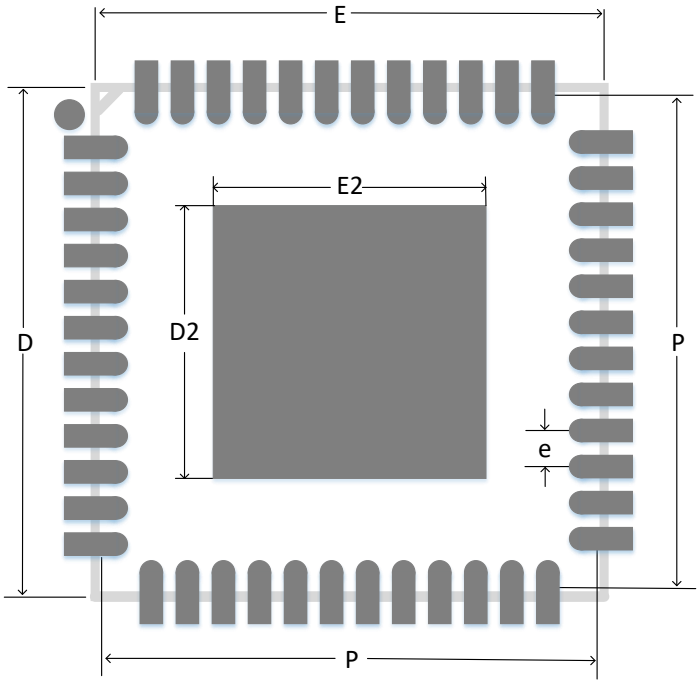
4.1 QN48 Package Outline (6mm x 6mm)

Figure 4-1 Package Outline QN48



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 4-2 Recommended PCB Layout QN48



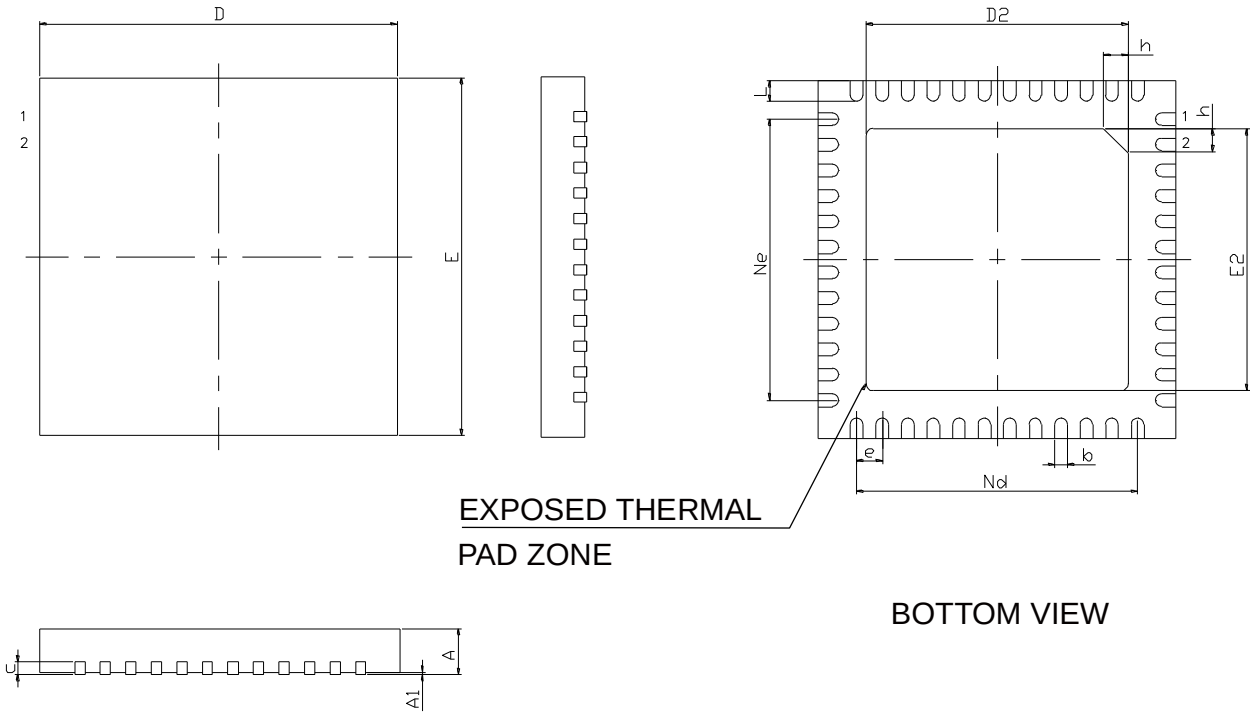
TOP VIEW

Unit:mm

D	6.00
E	6.00
D2	4.3
E2	4.3
P	5.90
e	0.40
L	0.85
b	0.20

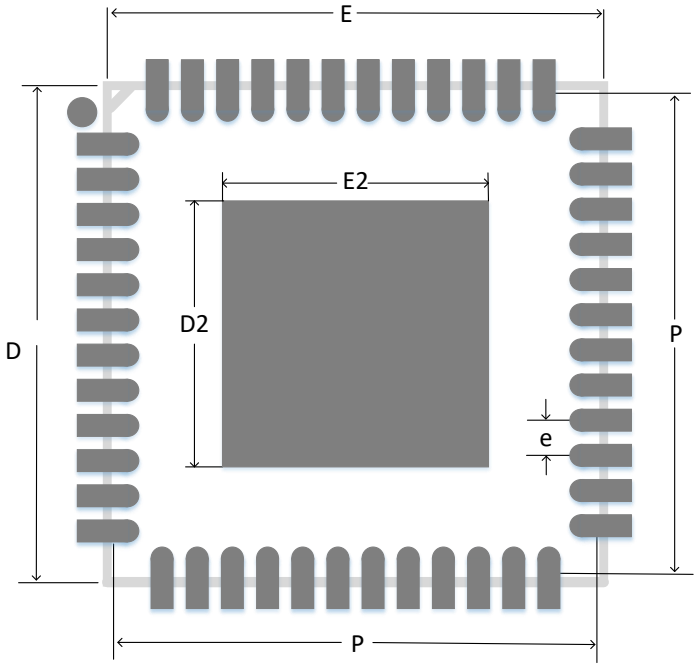
4.2 QN48E Package Outline (6mm x 6mm)

Figure 4-3 Package Outline QN48E



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.75	0.85	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Figure 4-4 Recommended PCB Layout QN48E



Unit:mm

D	6.00
E	6.00
D2	4.3
E2	4.3
P	5.90
e	0.40
L	0.85
b	0.20

GOWIN
PROGRAMMING FOR THE FUTURE