DK_MINI_GW1N-LV4LQ144C6I5_V1.1

User Guide

DBUG383-1.0E, 01/18/2021

Disclaimer

Revision History

Date	Version	Description
01/18/2021	1.0E	Initial version published.

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1 About This Guide

1.1 Purpose

The DK_MINI_GW1N-LV4LQ144C6I5_V1.1 user manual consists of the following four parts:

1. A brief introduction to the features and hardware resources of the development board;
2. An introduction to the function, circuit, and pinout of each module;
3. Notes for the use of the development board:
4. An introduction to the usage of the FPGA development software.

1.2 Supported Products

The information in the guide applies to GW1N series of FPGA products: GW1N-4.

1.3 Related Documents

You can find the related documents at www.gowinsemi.com:

- DS100, GW1N series of FPGA Products Data Sheet
- UG103, GW1N series of FPGA Products Package and Pinout
- UG105, GW1N-4 Pinout
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- SUG100, Gowin Software User Guide

1.4 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
LED	Light Emitting Diode
LDO	Low Dropout Regulator
GPIO	Gowin Programmable Input/Output
LUT4	4-input Look-up Tables
SSRAM	Shadow Static Random Access Memory
BSRAM	Block Static Random Access Memory
PLL	Phase-locked Loop
DLL	Delay-locked Loop
DSP	Digital Signal Processing
LQ144	LQFP144 package

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

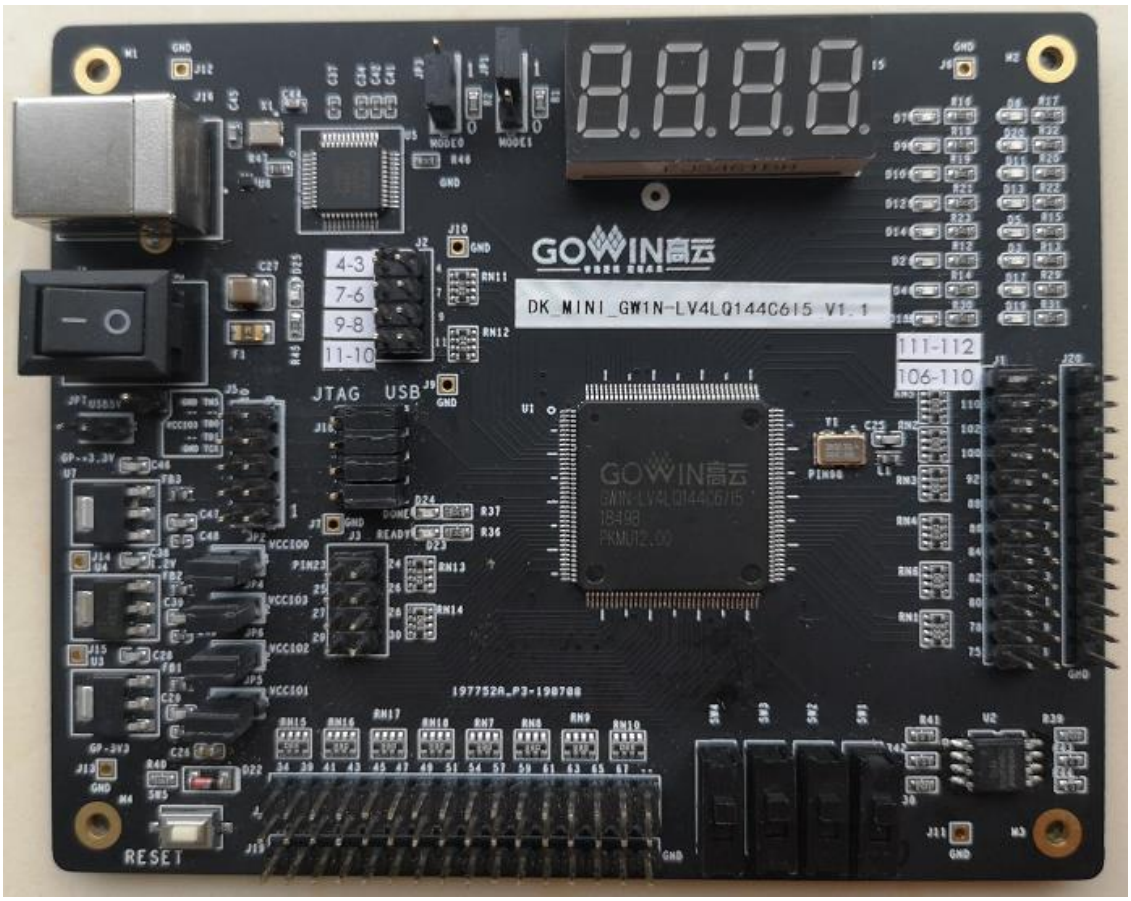
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Description

2.1 Overview

Figure 2-1 Development Board



The Development board adopts the GW1N-4 devices of the GW1N series of FPGA products. It features a range of advanced features including low power consumption, instant start-up, high security, low-cost, and flexible extensions, all of which can effectively reduce the learning cost and help users quickly design and develop programmable logic devices.

The development board offers 4 interfaces, GPIO interface, SPMI, keys, LEDs, etc., which is useful for both developers and learners.

2.2 Development Kit

A development board kit includes the following items:

- Development Board
- USB Cable

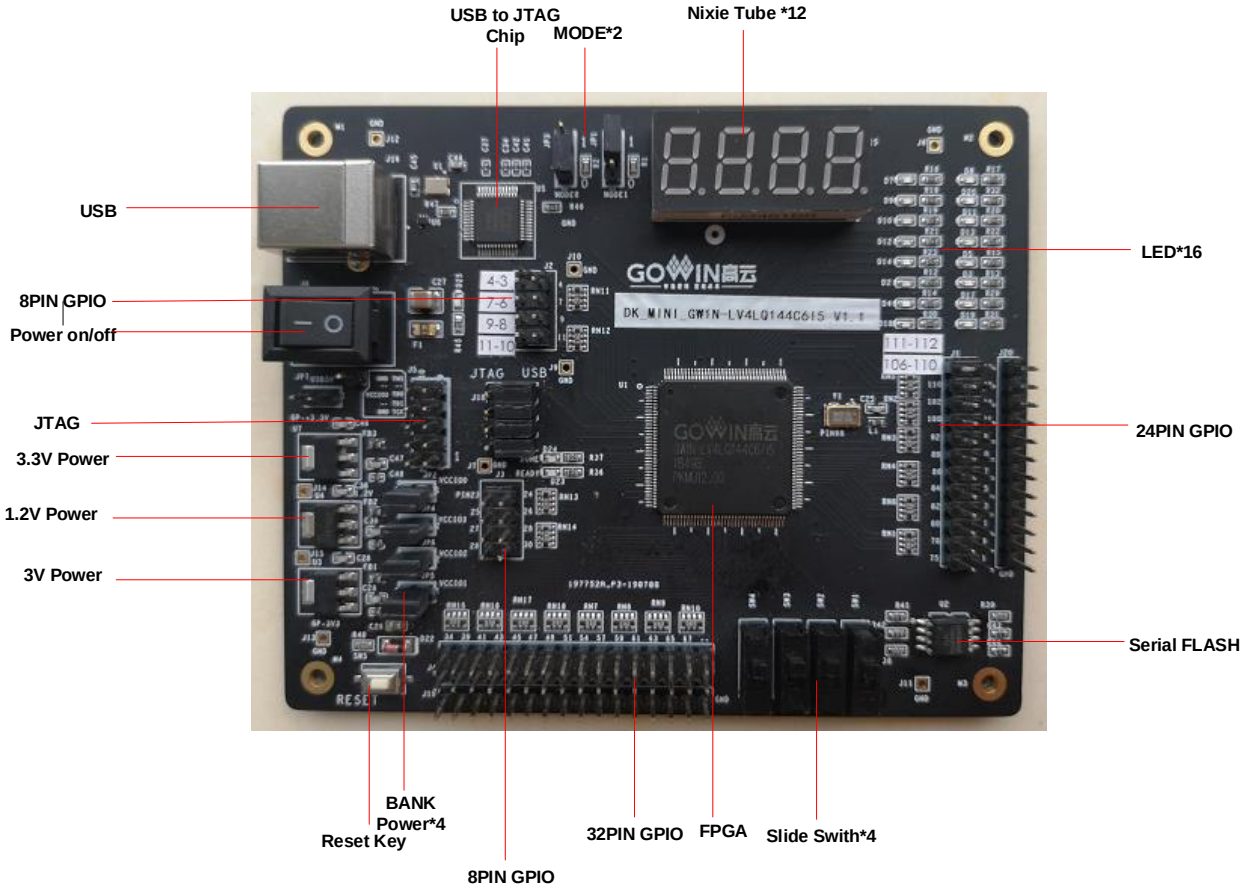
Figure 2-2 A Development Kit

① Development Board

② USB Cable

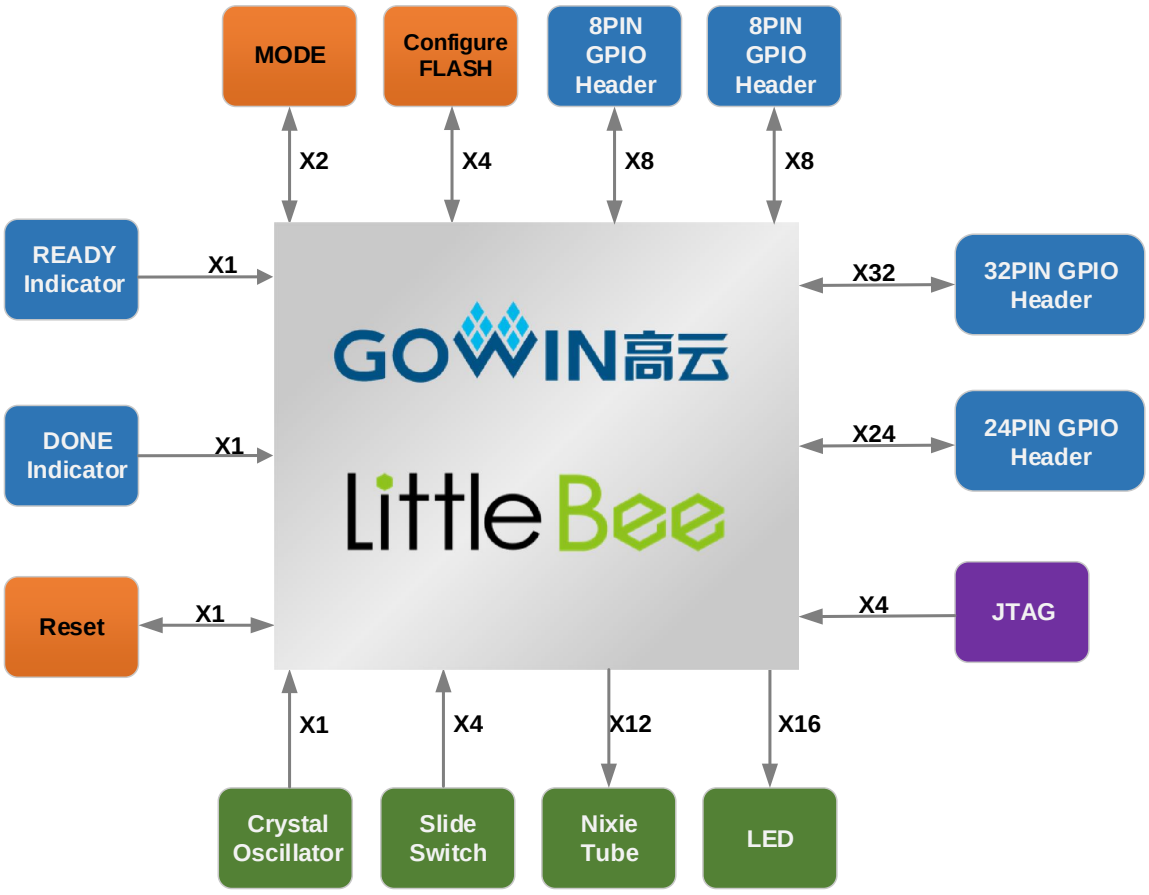
2.3 PCB Components

Figure 2-3 PCB Components



2.4 System Block Diagram

Figure 2-4 System Block Diagram



2.5 Features

The features of the development board are as follows:

1. FPGA
   - LQFP144 package
   - Embedded flash, data does not easily lost if power down.
   - Abundant LUT4 resources
   - Multiple modes and capacities of B-SRAM
   - Supports LV
2. FPGA Configuration Mode
   - JTAG, AUTO BOOT, MSPI
3. Clock resource
   - 50MHz clock crystal oscillator
4. Key switch and slide switch
   - One reset key
   - Four Slide switches
5. LED
   - One Power indicator (green)

- One DONE indicator (green)
- One READY indicator (green)
- 16 LEDs (green)
- One digital tube

6. Memory
   - 64Mbit SPI Flash
7. GPIO
   - 72 I/Os
8. LDO Power
   - Inverse voltage protection, overcurrent protection
   - Supports 3.3 V, 3V, and1.2V

2.6 Development Board Description

Table 2-1 Development Board Description

No.	Name	Functional Description	Conditions	Remarks
1	FPGA	Core chip	–	–
2	Download	Supports USB interface; Supports JTAG, AUTOBOOT, MSPI.	Supports USB to JTAG module	–
3	Power Supply	Provides USB5V input, and 3.3 V, 3V and 1.2 V output via LDO circuit	Input power: 5V 5V to 3.3V, 3V circuit provides power for FPGA, download circuit and other circuits. 5V to 1.8V circuit provides power for FPGA.	–
4	Slide switches	Available for testing	Four	–
5	Reset key	FPGA reset	One	–
6	LED	Test indicator, DONE indicator, READY indicator, and Power indicator.	Sixteen test indicators, green; One DONE indicator, green. One Power indicator, green. One READY indicator, green.	–
7	Crystal Oscillator	Provides 50MHz clock for FPGA	Package5032	–
8	GPIO	For extending and testing	Seventy-two with 3.3V	–
9	Digital tube	For testing	One	–
10	Protection	USB interface: ESD protection; Power interface: Inverse current and over current protection	USB interface with ESD protection: ±15kV non-contact discharge and ± 8kV contact discharge; Schottky diode is connected between positive and negative anodes of power interface; 2A self-recovery fuses are connected at power input.	–
11	Voltage	–	Input: 2.7V~5.5V	–
12	Humidity	–	95%	–
13	Temperature	–	Operating range: –20°~70°	–

3 FPGA Circuits

3.1 FPGA Module

Overview

For the resources of GW1N series of FPGA Products, please refer to DS100, GW1N series of FPGA Products Data Sheet.

I/O BANK Introduction

For the I/O BANK, package and pinout information, see UG103, GW1N series of FPGA Products Package and Pinout for more details.

3.2 Download

3.2.1 Overview

The development board provides USB download interface and also JTAG download. J5 is the JTAG download port, and J18 can select JTAG and USB download mode by short circuit cap.

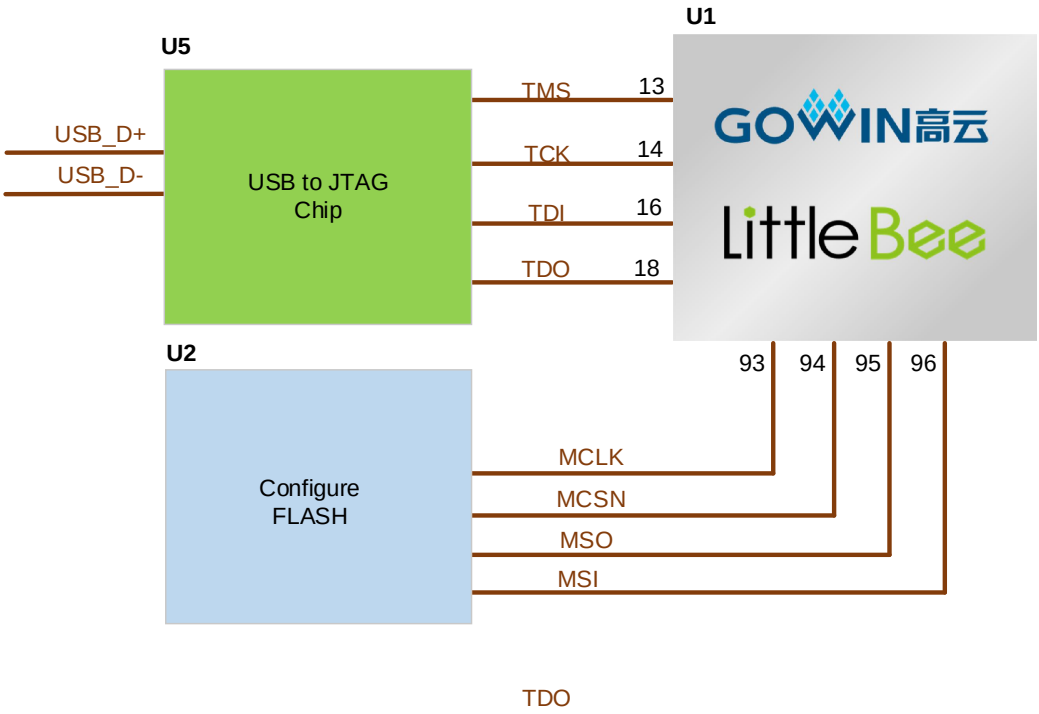
The data stream file can be downloaded to the internal SRAM, internal flash, or external flash as needed.

Note!

- When downloaded to SRAM, the bitstream file will be lost if the device is powered down, and it will need to be downloaded again after power-on.
- If downloaded to flash, the bitstream file will not be lost if the device is powered down.

3.2.2 USB Download Circuit

Figure 3-1 Connection Diagram of FPGA USB Downloading and Configuration



3.2.3 Download Flow

The bitstream file can be downloaded in the following ways:

1. SRAM:
   SRAM: Scan the device and download bitstream after power on. When Done is on, it indicates it is successful.
   Note!
   The mode is independent of the values of MODE0 and MODE1.
2. Internal Flash:
   Power on and download. After downloading the data stream file successfully, power down to reset and load the bit file from the internal Flash, and when the Done indicator lights up to denote that the download has been successful.
   Note!
   When downloading and starting internal FLASH, you need to set MODE0 and MODE1 to "00".
3. External Flash:

   Power on to download. Power down to reset and load the bit file from the external flash. The Done indicator lights up to denote that the download has been successful.

   Note!

- When downloading external FLASH, MODE0 and MODE1 need to set to "1" and "1".
- When loading extrnal Flash, MODE0 and MODE1 need to set to "0" and "1".

3.2.4 Pinout

Table 3-1 FPGA Pinout

Name	Pin No.	BANK	Description	I/O Level
TMS	13	3	JTAG signal	VCCO3
TCK	14	3	JTAG Signal	VCCO3
TDI	16	3	JTAG Signal	VCCO3
TDO	18	3	JTAG Signal	VCCO3
MCLK	93	1	Configure FLASH Signal	VCCO1
MCSN	94	1	Configure FLASH Signal	VCCO1
MSO	95	1	Configure FLASH Signal	VCCO1
MSI	96	1	Configure FLASH Signal	VCCO1

3.3 Power Supply

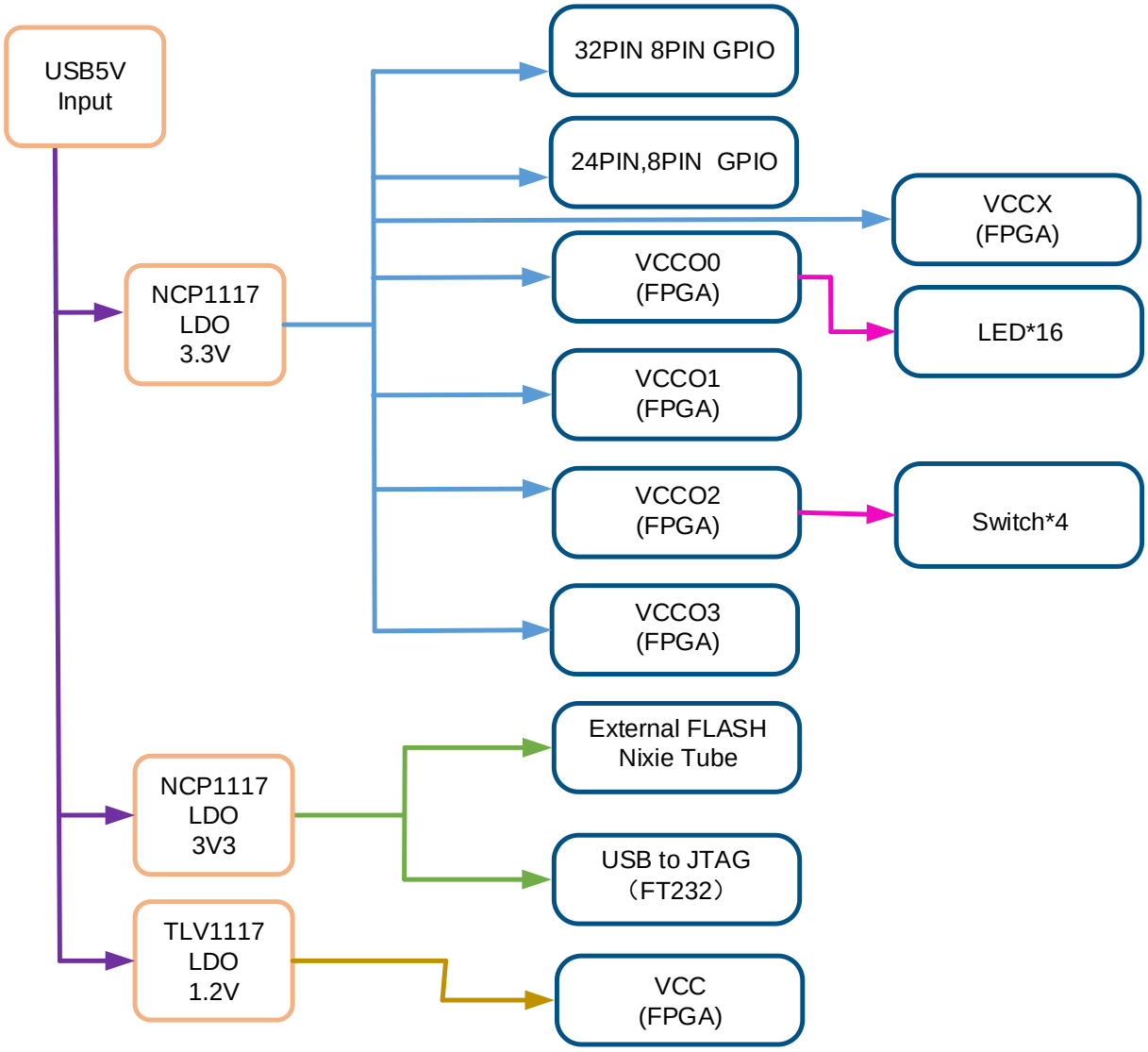
3.3.1 Overview

The power is supplied by USB5V or JP7), and the interface has overcurrent and inverse current protection. The overcurrent limit is 2A.

The LDO power supply chip is used to step down voltage from 5V to 3.3V, 2.5V, and 2V; power supply can support up to 1A, which can meet the power demand of the development board.

3.3.2 Power System Distribution

Figure 3-2 Power System Distribution



3.3.3 Pinout

Table 3-2 GW1N-4 FPGA Power Pinout

Name	Pin No.	BANK	Description	I/O Level
VCCO0	109, 127	0	I/O Bank Voltage	3.3V
VCCO1	77, 91	1	I/O Bank Voltage	3.3V
VCCO2	37, 55	2	I/O Bank Voltage	3.3V
VCCO3	5, 19	3	I/O Bank Voltage	3.3V
VCCX	31, 103	-	Auxiliary voltage	3.3V
VCC	1, 36, 73, 108	-	Core voltage	1.2V
VSS	2, 17, 33, 35, 53, 74, 89, 105, 107, 125	-	GND	-

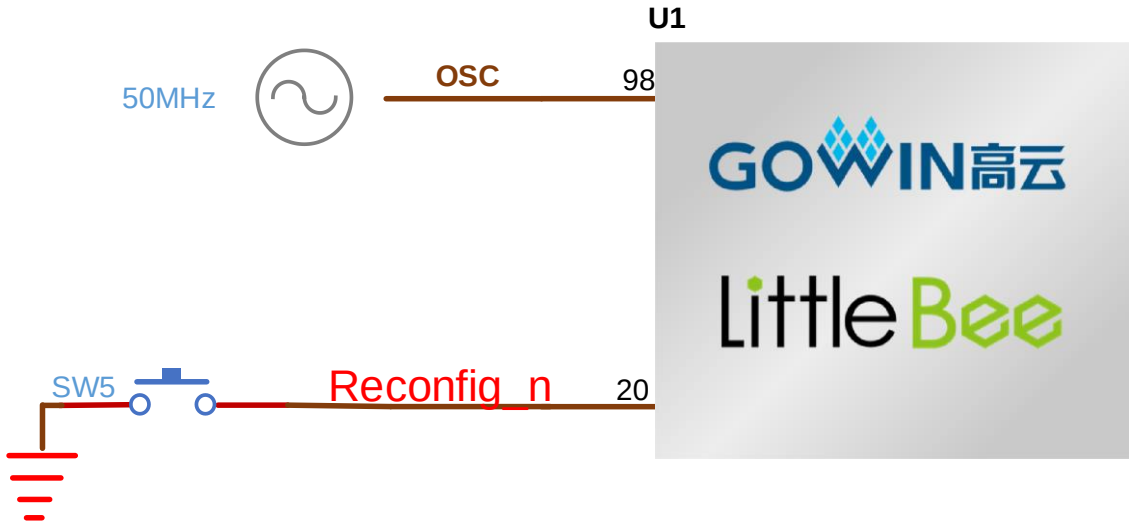
3.4 Clock, Reset

3.4.1 Overview

The development board offers a 50MHz oscillator, connecting to the 98 pin.

3.4.2 Clock, Reset Circuit

Figure 3-3 Clock, Reset Circuit



3.4.3 Pinout

Table 3-3 FPGA Clock and Reset Pinout

Name	Pin No.	BANK	Description	I/O Level
OSC	98	1	50MHz crystal oscillator input	3.3V
Reconfig_n	20	3	Reset Signal, active-low	3.3V

3.5 LED

3.5.1 Overview

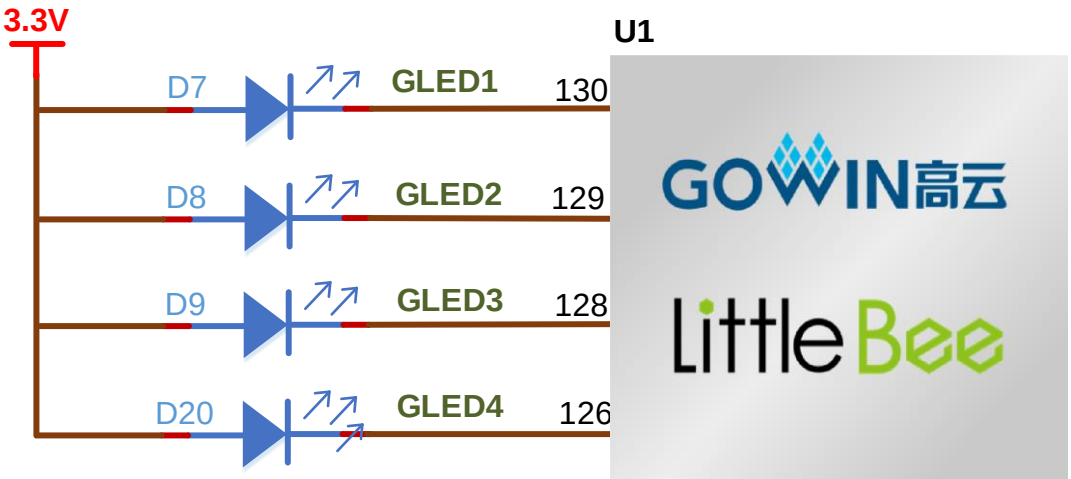
There are sixteen green LEDs on the development board and the LED can display the required status. In addition, two LEDs are reserved to indicate the power supply and FPGA loading status.

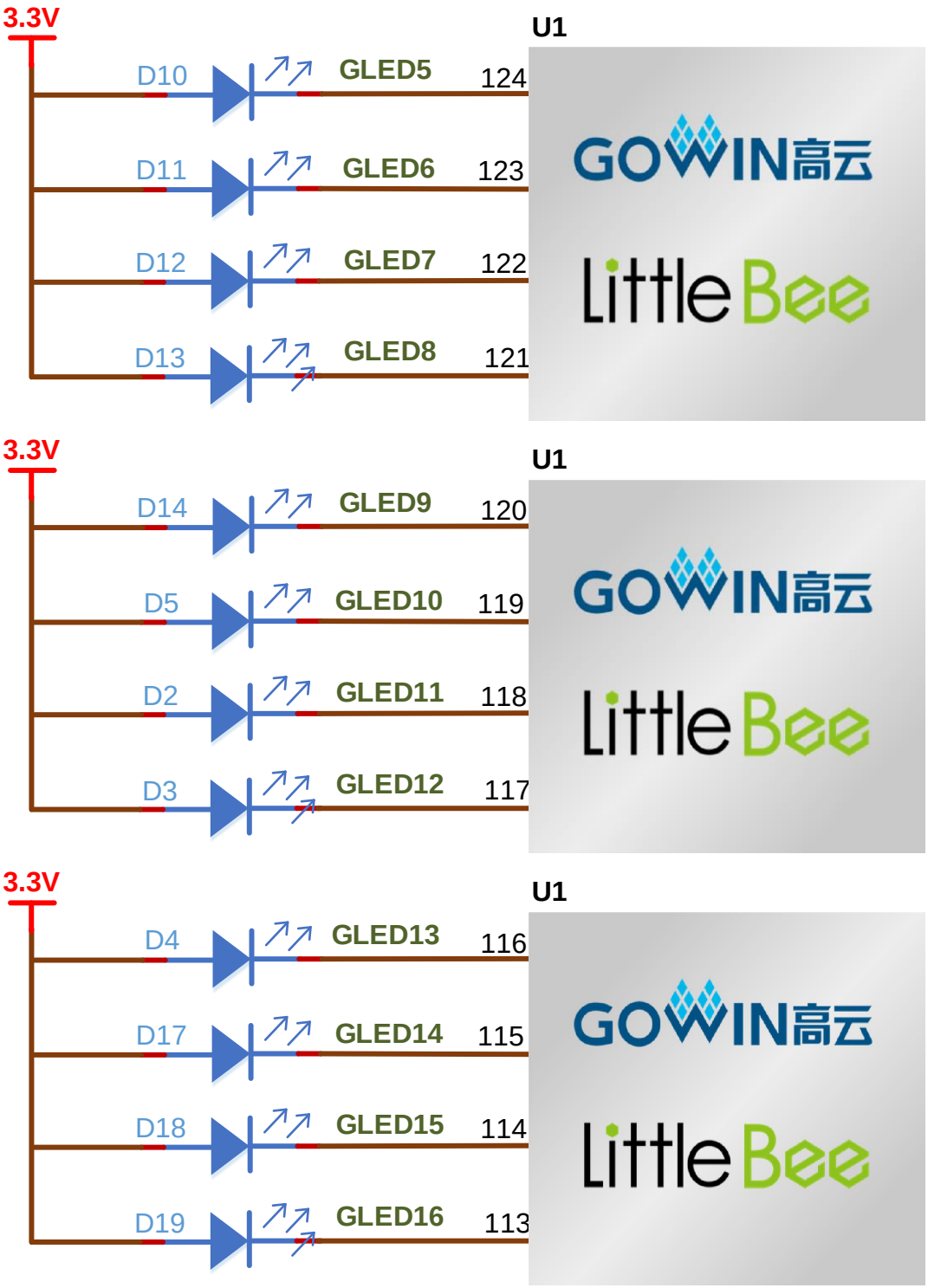
You can test the LEDs in the following ways:

- When the FPGA corresponding pin output signal is logic low , the LED is lit;
- If the signal is high, LED is off.

3.5.2 LED Circuit

Figure 3-4 LED Circuit




3.3V
U1
D10
GLED5
124
D11
GLED6
123
D12
GLED7
122
D13
GLED8
121
3.3V
U1
D14
GLED9
120
D5
GLED10
119
D2
GLED11
118
D3
GLED12
117
3.3V
U1
D4
GLED13
116
D17
GLED14
115
D18
GLED15
114
D19
GLED16
113

3.5.3 Pinout

Table 3-4 LED Pinout

Name	Pin No.	BANK	Description	I/O Level
GLED_1	130	0	LED 1	3.3V
GLED_2	129	0	LED 2	3.3V
GLED_3	128	0	LED 3	3.3V
GLED_4	126	0	LED 4	3.3V
GLED_5	124	0	LED 5	3.3V
GLED_6	123	0	LED 6	3.3V
GLED_7	122	0	LED 7	3.3V
GLED_8	121	0	LED 8	3.3V
GLED_9	120	0	LED 9	3.3V
GLED_10	119	0	LED 10	3.3V
GLED_11	118	0	LED 11	3.3V
GLED_12	117	0	LED 12	3.3V
GLED_13	116	0	LED 13	3.3V
GLED_14	115	0	LED 14	3.3V
GLED_15	114	0	LED 15	3.3V
GLED_16	113	0	LED 16	3.3V

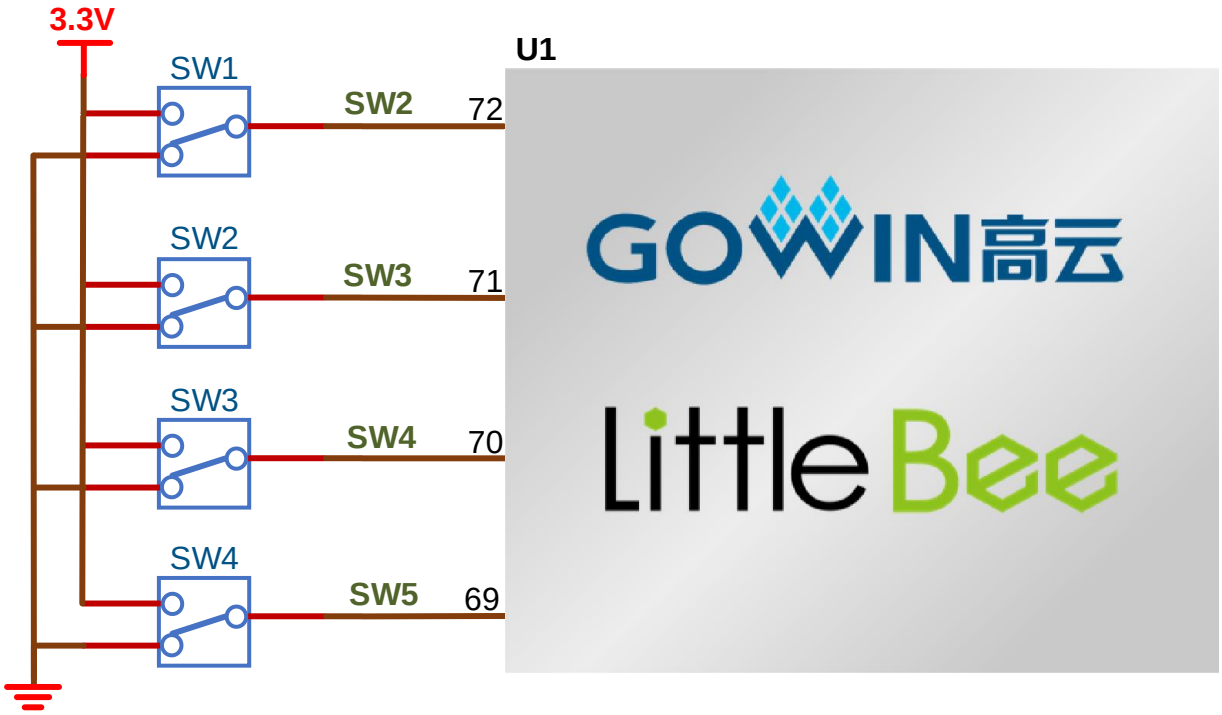
3.6 Switches

3.6.1 Overview

There are four slide switches in the development board to control input during testing.

3.6.2 Switch Circuit

Figure 3-5 Switches Circuit



3.6.3 Pinout

Table 3-5 Switch Circuit Pinout

Name	Pin No.	BANK	Description	I/O Level
SW2	72	2	Slide Switch1	3.3V
SW3	71	2	Slide Switch2	3.3V
SW4	70	2	Slide Switch3	3.3V
SW5	69	2	Slide Switch4	3.3V

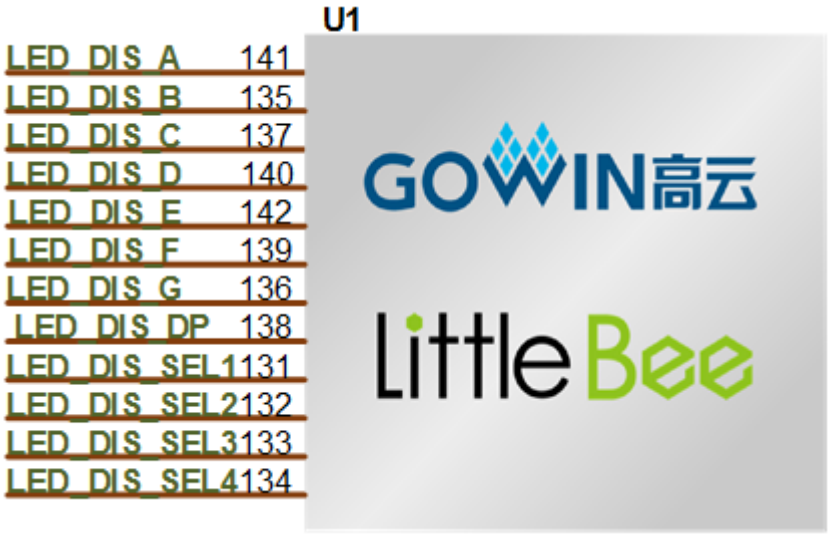
3.7 Digital tube

3.7.1 Overview

The development board has a 4-digit tube, and you can control the display through the sequence, which is used for simple function test.

3.7.2 Digital Tube Circuit

Figure 3-6 Digital Tube Circuit



3.7.3 Pinout

Table 3-6 Clock Circuit Tube Pinout

Name	Pin No.	BANK	Description	I/O Level
LED_DIS_A	141	0		3.3V
LED_DIS_B	135	0		3.3V
LED_DIS_C	137	0		3.3V
LED_DIS_D	140	0		3.3V
LED_DIS_E	142	0		3.3V
LED_DIS_F	139	0		3.3V
LED_DIS_G	136	0		3.3V
LED_DIS_DP	138	0		3.3V
LED_DIS_SEL1	131	0		3.3V
LED_DIS_SEL2	132	0		3.3V
LED_DIS_SEL3	133	0		3.3V
LED_DIS_SEL4	134	0		3.3V

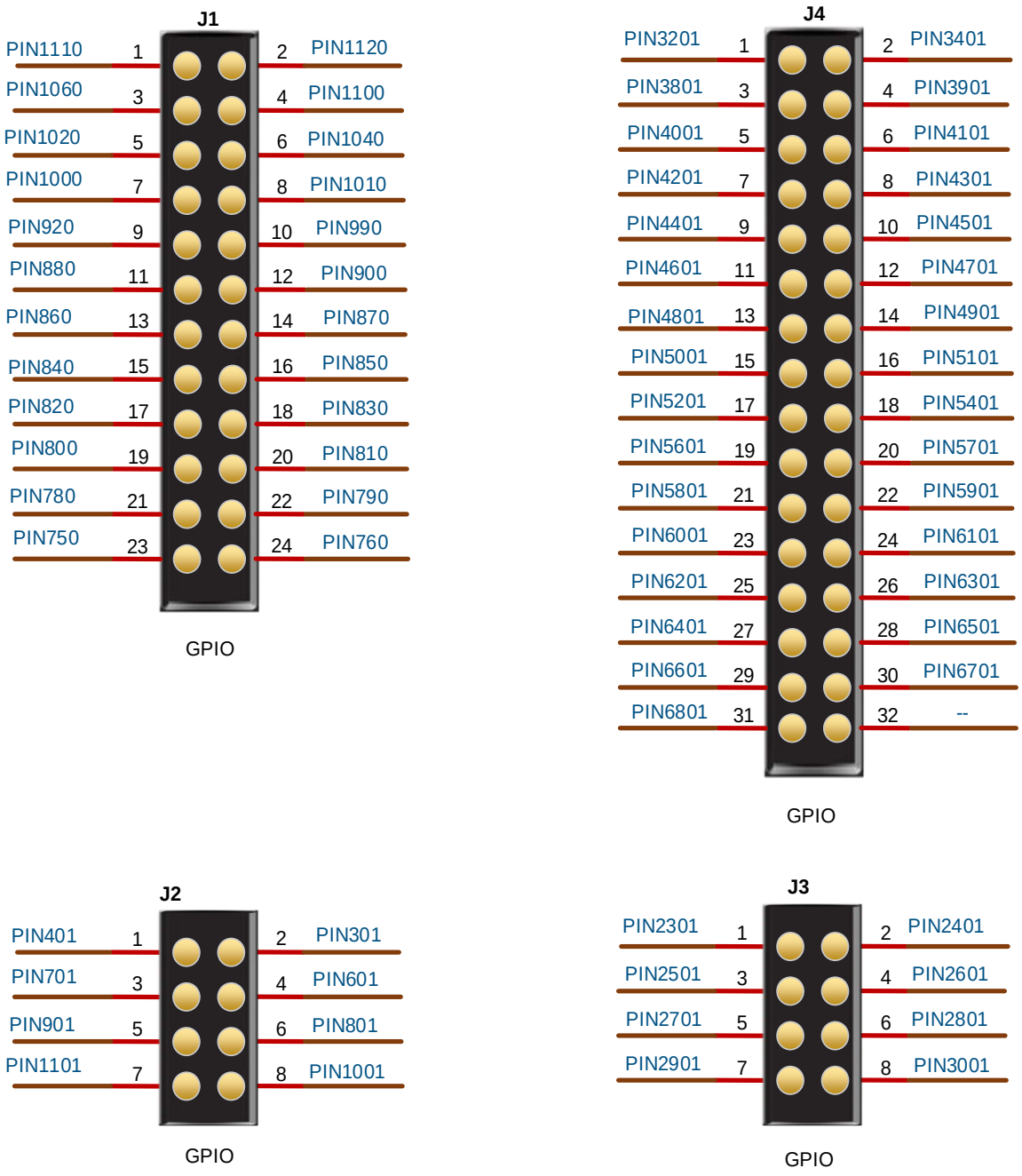
3.8 GPIO

3.8.1 Overview

Four 2.54mm pins are reserved on the development board for function extension and testing

3.8.2 GPIO Circuit

Figure 3-7 GPIO Circuit



3.8.3 Pinout

The pinout of the J1 FPGA and J4 FPGA are listed in Table 3-7 and Table 3-8.

Table 3-7 J1 FPGA Pinout

Name	Pin No.	24P Socket Pin No.	BANK	Description	I/O Level
PIN1110	111	1	0	General I/O	3.3V
PIN1120	112	2	0	General I/O	3.3V
PIN1060	106	3	1	General I/O	3.3V
PIN1100	110	4	0	General I/O	3.3V
PIN1020	102	5	1	General I/O	3.3V
PIN1040	104	6	1	General I/O	3.3V
PIN1000	100	7	1	General I/O	3.3V
PIN1010	101	8	1	General I/O	3.3V
PIN920	92	9	1	General I/O	3.3V
PIN990	99	10	1	General I/O	3.3V
PIN880	88	11	1	General I/O	3.3V
PIN900	90	12	1	General I/O	3.3V
PIN860	86	13	1	General I/O	3.3V
PIN870	87	14	1	General I/O	3.3V
PIN840	84	15	1	General I/O	3.3V
PIN850	85	16	1	General I/O	3.3V
PIN820	82	17	1	General I/O	3.3V
PIN830	83	18	1	General I/O	3.3V
PIN800	80	19	1	General I/O	3.3V
PIN810	81	20	1	General I/O	3.3V
PIN780	78	21	2	General I/O	3.3V
PIN790	79	22	1	General I/O	3.3V
PIN750	75	23	2	General I/O	3.3V
PIN760	76	24	2	General I/O	3.3V

Table 3-8 J4 FPGA Pinout

Name	Pin No.	32P Socket Pin No.	BANK	Description	I/O Level
PIN3201	32	1	2	General I/O	3.3V
PIN3401	34	2	2	General I/O	3.3V
PIN3801	38	3	2	General I/O	3.3V
PIN3901	39	4	2	General I/O	3.3V
PIN4001	40	5	2	General I/O	3.3V
PIN4101	41	6	2	General I/O	3.3V
PIN4201	42	7	2	General I/O	3.3V

Name	Pin No.	32P Socket Pin No.	BANK	Description	I/O Level
PIN4301	43	8	2	General I/O	3.3V
PIN4401	44	9	2	General I/O	3.3V
PIN4501	45	10	2	General I/O	3.3V
PIN4601	46	11	2	General I/O	3.3V
PIN4701	47	12	2	General I/O	3.3V
PIN4801	48	13	2	General I/O	3.3V
PIN4901	49	14	2	General I/O	3.3V
PIN5001	50	15	2	General I/O	3.3V
PIN5101	51	16	2	General I/O	3.3V
PIN5201	52	17	2	General I/O	
PIN5401	54	18	2	General I/O	3.3V
PIN5601	56	19	2	General I/O	3.3V
PIN5701	57	20	2	General I/O	3.3V
PIN5801	58	21	2	General I/O	3.3V
PIN5901	59	22	2	General I/O	3.3V
PIN6001	60	23	2	General I/O	3.3V
PIN6101	61	24	2	General I/O	3.3V
PIN6201	62	25	2	General I/O	3.3V
PIN6301	63	26	2	General I/O	3.3V
PIN6401	64	27	2	General I/O	3.3V
PIN6501	65	28	2	General I/O	3.3V
PIN6601	66	29	2	General I/O	3.3V
PIN6701	67	30	2	General I/O	3.3V
PIN6801	68	31	2	General I/O	3.3V
--		32	--	General I/O	3.3V

The pinout of the J2 FPGA and J4 FPGA are listed in Table 3-9 and Table 3-10.

Table 3-9 J2 FPGA Pinout

Name	Pin No.	8P Socket Pin No.	BANK	Description	I/O Level
PIN401	4	1	3	General I/O	3.3V
PIN301	3	2	3	General I/O	3.3V
PIN701	7	3	3	General I/O	3.3V
PIN601	6	4	3	General I/O	3.3V
PIN901	9	5	3	General I/O	3.3V
PIN801	8	6	3	General I/O	3.3V
PIN1101	11	7	3	General I/O	3.3V
PIN1001	10	8	3	General I/O	3.3V

Table 3-10 J3 FPGA Pinout

Name	Pin No.	8P Socket Pin No.	BANK	Description	I/O Level
PIN2301	23	1	3	General I/O	3.3V
PIN2401	24	2	3	General I/O	3.3V
PIN2501	25	3	3	General I/O	3.3V
PIN2601	26	4	3	General I/O	3.3V
PIN2701	27	5	3	General I/O	3.3V
PIN2801	28	6	3	General I/O	3.3V
PIN2901	29	7	3	General I/O	3.3V
PIN3001	30	8	3	General I/O	3.3V

4 Notes

Notes for using the development board:

- Handle with care and pay attention to electrostatic protection.
- When downloading bitstream files to internal flash or external flash, set the MODE pin to correct configuration value. Please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide for details;
- The power DC5V is input by USB port or JP7.
- The VCCO power of the four banks of the FPGA can be directly connected to 3.3V through JP2, JP4, JP5 and JP6 pins, or the required voltage can be supplied externally.

5 Gowin Software

For the details, you can see SUG100, Gowin Software User Guide.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