



Gowin LVDS7:1 LCD Driver Controller Reference Design **User Guide**

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Revision History

| Date | Version | Description |
|------------|---------|------------------|
| 12/20/2017 | 1.00E | Initial version. |

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1 About This Guide

1.1 Purpose

This guide describes LVDS7:1 LCD Driver Controller Reference Design. It mainly documents its functions and features, ports and timing etc., which helps users to quickly understand features and usage of Gowin LVDS7:1 LCD Driver Controller Reference Design.

1.2 Supported Products

The information in the guide applies to the following products:

GW2AR series FPGA products: GW2AR-18

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents via <http://www.gowinsemi.com.cn>:

GW2AR series FPGA Products Data Sheet

1.4 Abbreviation and Terminology

The abbreviations and terminologies used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

| Abbreviations and Terminology | Full Name | Meaning |
|-------------------------------|------------------------------------|------------------------------------|
| FPGA | Field Programmable Gate Array | Field Programmable Gate Array |
| LVDS | Low-Voltage Differential Signaling | Low-Voltage Differential Signaling |
| I/O | Input/Output | Input/Output |
| PLL | Phase Locked Loop | PLL |

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

Website: <http://www.gowinsemi.com.cn>

E-mail: support@gowinsemi.com

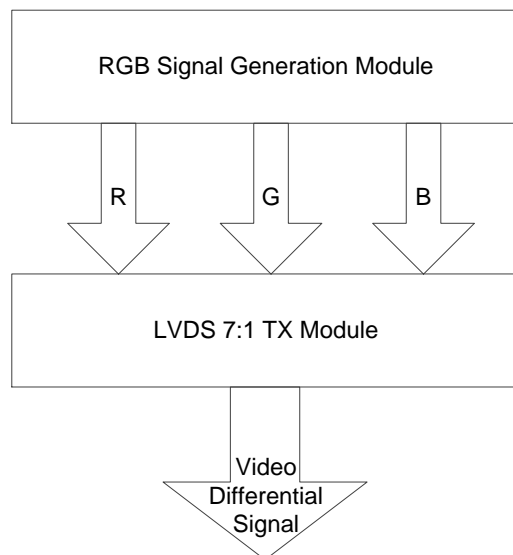
+Tel: +86 755 8262 0391

2Overview

2.1 Introduction

As a core block of the LCD driver circuit, the LCD driver controller provides timing signals and displays data for LCD display system which is the port between the company and LCD display system. In LVDS7:1 LCD Driver Controller Reference Design, the port adopts LVDS I/O standard and the RGB signal can be converted to the standard video difference signal. The structure diagram is shown as Figure 2-1.

Figure 2-1 LVDS7:1 LCD Driver Controller Schematic View



3 Features and Performance

3.1 Key Features

- Comply with LVDS port standard;
- Adopt low-voltage differential signaling;
- Support transfer data with the high speed, low noise, long distance and high accuracy.

3.2 Max. Frequency

The frequency of LVDS7:1 LCD Driver Controller Reference Design timing port can be up to 800 MBPS.

3.3 Resource Utilization

LVDS7:1 LCD Driver Controller can be realized via Verilog which is applied to GW2A-18-LQFP144 FPGA. Resource utilization is as shown in Table 1.

Table 1 Resource Utilization

| Package Information | Speed Grade | Name | Resource Utilization |
|---------------------|-------------|--------|----------------------|
| GW2AR-18-LQFP144 | -8 | LUT | 85 |
| | | ALU | 30 |
| | | PLL | 1 |
| | | CLKDIV | 1 |
| | | REG | 46 |

4 Functional Description

4.1 Functions

LVDS7:1 LCD Driver Controller Reference Design includes 2 modules:

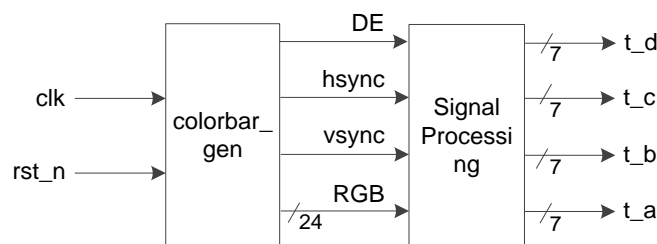
- RGB signal generation module
- LVDS 7:1 TX module

RGB signal generation module mainly provides 24-bit RGB signal, line / field synchronizing signal and enable control signal; LVDS 7:1 TX module converts the 4-channel 7-bit LVDS signal to the 4-channel series signal that can drive the LCD.

4.2 RGB Signal Generation Module

RGB signal generation module provides 24-bit RGB signal, line / field synchronizing signal and converts these signals to the 4-channel 7-bit LVDS signals. Functional digram of RGB signal generation module is as shown in Figure 4-1.

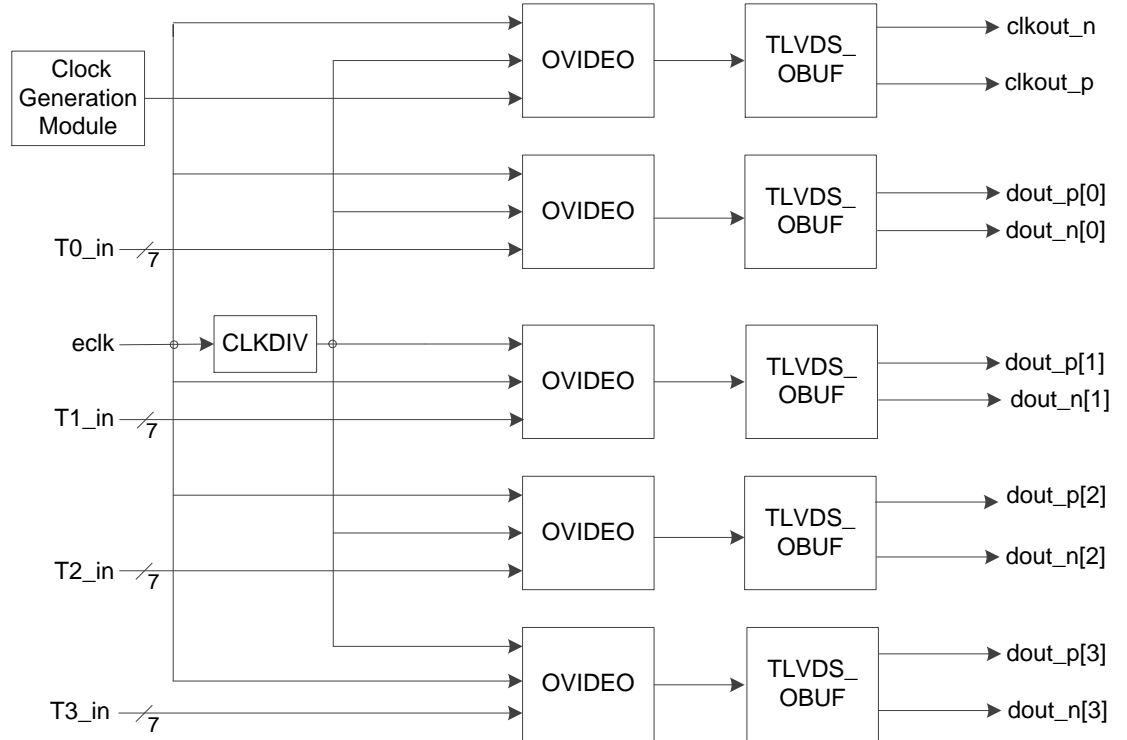
Figure 4-1 Functional Digram of Signal Generation Module



4.3 LVDS 7:1 TX Module

LVDS 7:1 TX module converts the 4-channel 7-bit LVDS signal received from RGB generation module to the 4-channel series signal for driving the LCD. Functional diagram is as shown in Figure 4-2.

Figure 4-2 Functional diagram of LVDS 7:1 TX Module

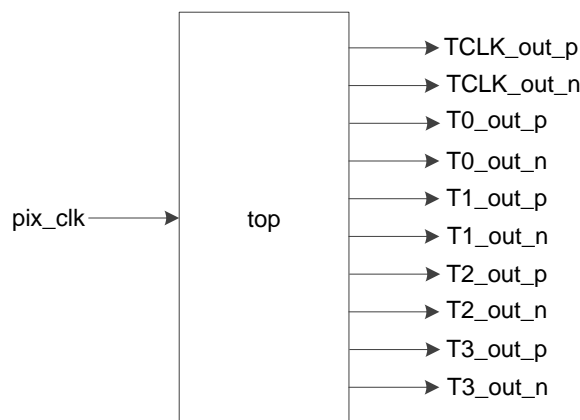


5 Ports Description

5.1 LVDS7:1 Driver Controller View

Ports Diagram of LVDS7:1 Driver Controller Reference Design is shown in Figure 5-1.

Figure 5-1 LVDS7:1 Driver Controller View



5.2 Port Signal

Ports signal of LVDS7:1 Driver Controller Reference Design is shown in Table 5-1.

Table 5-1 Ports Signal of LVDS7:1 Driver Controller Reference Design

| Port Name | Port Type | Description |
|------------|-----------|--------------------------------------------|
| pix_clk | input | Clocksignal |
| TCLK_out_p | output | Synchronous clock source CLK |
| TCLK_out_n | output | Synchronous clock source CLK |
| T0_out_p | output | Output serial data at port TX Of 0-channel |
| T0_out_n | output | Output serial data at port TX Of 0-channel |

| Port Name | Port Type | Description |
|-----------|-----------|--------------------------------------------|
| T1_out_p | output | Output serial data at port TX of 1-channel |
| T1_out_n | output | Output serial data at port TX of 1-channel |
| T2_out_p | output | Output serial data at port TX of 2-channel |
| T2_out_n | output | Output serial data at port TX of 2-channel |
| T3_out_p | output | Output serial data at port TX of 3-channel |
| T3_out_n | output | Output serial data at port TX of 3-channel |

6 Timing Description

This chapter introduces the output signal timing of LVDS7:1 Driver Controller Reference Design.

6.1 Timing Port Requirement

LVDS7:1 Driver Controller Reference Design is used for producing a RGB signal and sending to the LCD after the signal is being converted to the standard video differential signal. The video differential signal includes the 1-channel (TCLK_out) and the 4-channel (T0_out, T1_out, T2_out and T3_out). A pair of differential data line can transmit 7-bit data. The signal timing is as shown in Figure 6-1.

Figure 6-1 LVDS7:1 Driver Port Timing

