GW1N series FPGA Products Principle Diagram Guide

Introduction

A series of rules for circuit board design should be followed when using GW1N series FPGA products. This manual describes characteristics and special usages of the GW1N series FPGA products, and provides a checklist table for guiding principle diagram design. The main contents are as follows:

- Power Management
- Configuration Modes Selection
- Pin Distribution

GW1N series FPGA products support both lower voltage(LV) and upper voltage(UV) with the features of low power, instant on, and non-volatile. LV supports 1.2 V core voltage; UV supports 1.8V, 2.5V, and 3.3V core voltage, and has built-in linear voltage regulator. LV and UV have the same functions, and the pins are compatible.

Power Management

Core voltagesV_{CC} and V_{CCO3} are used for internal power-on reset/set in GW1N series FPGA products. V_{CCO0} ~ V_{CCO2} are used to power up the other IO BANKs. The device can work normally only if power supply voltages reaches the recommended working range.Table 1 lists the recommended working range of each power voltage.

Table 1 Recommended Working Range

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
V_{CCO}	I/O Bank Power	1.14V	3.6V
V_{CCX}	Auxiliary Power	2.3V	3.465V

For specific density, packages, and resource utilization, GPA tools can be used to evaluate and analyze power consumption.

Configuration Modes Selection

GW1N series FPGA products include SRAM and Flash.

- Volatile SRAM is provided for running valid configuration files;
- Non-volatile Flash is used to store configuration files and can configure SRAM.

GW1N series FPGA products support multiple programming and configuration interfaces: 1149.1 JTAG, auto-boot, slave SPI, master SPI, and dual boot.

It's recommended to reserve at least one programming and configuration interface. Programming and configuration interfaces are controlled through MODE pins, and the truth table is shown in Table 2.

Table 2 Configuration Mode

Configuration		MODE[2:0][1]	Instructions
JTAG		XXX[2]	GW1N series FPGA products are configured by hardware processor via JTAG interface.
GowinCONFIG	AUTO BOOT	000	GW1N series FPGA products are configured by reading data from built-in Flash
	SSPI	001	GW1N series FPGA products are configured by hardware processor via SPI interface.
	MSPI	010	As Master, GW1N series FPGA products are configured by reading data from external Flash (or other device) through SPI interface[3].
	DUAL BOOT	100	Read from built-in Flash first, and read from external Flash if built-in Flash configuration fails
	SERIAL[4]	101	GW1N series FPGA products are configured by hardware processor via DIN interface.
	CPU[4]	111	GW1N series FPGA products are configured by hardware processor via DBUS interface.

Note!

- [1] For some of the device packages all the MODE pins are not bonded out. The unbound Mode pins are grounded;
- [2] JTAG configuration MODE is independent of MODE input value;
- [3] SPI interfaces of SSPI and MSPI mode are independent of each other;
- [4] CPU configuration mode and SERIAL configuration mode share SCLK, WE_N and CLKHOLD_N; the data bus pins of CPU configuration mode share pins with those MSPI and SSPI configuration modes.

When programming and configuration pins are provided to interactive handshake with external devices, external matching resistance should be used. Please refer toTable 3 for Pull-Up 4.7 K or Pull-Down 1K resistance for different pins.

Table 3 Configuration Mode

Pin name	I/O	Description
RECONFIG_N	I, internal weak Pull-Up, external Pull-Up to V_{CCO3}	Low level pulse: start new GowinCONFIG configuration
READY	I/O, External Pull-Up to V_{CCO3}	High: the device can be programmed and configured currently
		Low: the device cannot be programmed and configured
DONE	External I/O Pull-Up to V_{CCO3}	High: successful completion of programming and configuration
		Low: unfinished or failure of programming and configuration
FASTRD_N /D3	I/O	In MSPI mode, FASTRD_N is used to select Flash access speed. Low: high speed Flash access mode High: regular Flash access mode
		Data port D3 in CPU mode
MCLK /D4	I/O, External Pull-Up 1 Ohm	Clock output MCLK in MSPI mode
		Data port D4 in CPU mode
MCS_N /D5	I/O, External Pull-Up to V_{CCO1}	MCS_N in MSPI mode, low-active
		Data port D5 in CPU mode
MI /D7	I/O	MISO in MSPI mode: Master data input/Slave data output
		Data port D7 in CPU mode
MO /D6	I/O	MISO in MSPI mode: Master data output/Slave data input
		Data port D6 in CPU mode
SSPI_CS_N/D0	I/O, External Pull-Up to V_{CCO1}	Enable signal SSPI_CS_N in SSPI mode, active-low, and weak pull-up inside
		Data port D0 in CPU mode
SO /D1	I/O	MISO in SSPI mode: Master data input/Slave data output
		Data port D1 in CPU mode
SI /D2	I/O	MISO in SSPI mode: Master data output/Slave data input
		Data port D2 in CPU mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I, External pull-down V_{CCO3}	Serial clock input in JTAG mode, which needs to be connected with 4.7 K pull-down resistance on PCB
TDI	I, internal weak pull-up	Serial data input in JTAG mode
TDO	O	Serial data output in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Select signal in JTAG mode, active low
SCLK	I, External I Pull-Up 1 Ohm	clock input in SSPI, SERIAL, CPU mode
DIN	I, internal weak pull-up	Input data in SERIAL mode
DOUT	O	Output data in SERIAL mode

Pin name	I/O	Description
CLKHOLD_N	I, internal weak pull-up	High: SCLK will be connected internally in SSPI mode or CPU mode
		Low: SCLK will be disconnected from SSPI mode or CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode

Master SPI mode should meet the following three points:

1. V_{CC} of SPI Flash and V_{CCO1} of GW1N series FPGA products should be consistent;
2. V_{CC} of SPI Flash should meet the range required in relevant manufacturers' data sheet;
3. POR level of SPI Flash should be lower than that of GW1N series FPGA product, which means SPI Flash will power up first.

Pin Distribution

Before designing circuit, FPGA pins distribution needs overall consideration. Make reasonable choices for applying device architecture features, including IO LOGIC, global clock resources, PLL resources, etc.

GW1N bank1/2/3 supports true LVDS output. When using true LVDS output, V_{CCO} shall be configured to 2.5 V or 3.3 V, and refer to *GW1N Series FPGA Product Pinout* to ensure that the corresponding pins support true LVDS output.

In order to support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as reference voltage. User can choose from internal reference voltage of the bank (0.5 x V_{CCO}) or external reference voltage using any IO from the bank.

Table 4 Checklist Table

	Checklist Items	OK	N/A
1	**Power Supply**		
1.1	LV Core voltage @ 1.2V		
1.2	UV Core voltage @ 1.8/2.5/3.3V		
1.3	1.2V~3.3V V_{CCO}0~3		
1.4	Power Estimation		
2	**Programming Configuration**		
2.1	Programming Configuration modes selection		
2.2	Pull-Up on SPI related pins		
2.3	Pull-Up on SPI related pins		
2.4	Pull-Down on JTAG TCK		
3	**Pin Distribution**		
3.1	True LVDS output pins support		
3.2	Reference voltage of SSTL, HSTL selection		

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

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Revision History

Date	Version	Description
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