GOWIN
PROGRAMMING FOR FUTURE

GW1N(R) series FPGA Products

# Programming and Configuration User Guide

**UG100-1.11E,6/1/2017**

## Disclaimer

## Revision History

| Date | Version | Description |
|---|---|---|
| 6/1/2017 | 1.11E | Initial Version. |

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# 1 About This Guide

## 1.1 Purpose

This manual describes GW1N(R) series FPGA products programming and configuration modes of Gowin (LittleBee®) family. Used together with *Gowin FPGA Products Programming and Configuration User Guide*, it helps you understand GW1N(R) series FPGA products configuration modes.

## 1.2 Supported Products

The information in the guide applies to the following products:

- GW1N series FPGA products: GW1N-1, GW1N-2, GW1N-4, GW1N-6, and GW1N-9.
- GW1NR series FPGA products: GW1NR-4, GW1NR-6, and GW1NR-9.

## 1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents at http://www.gowinsemi.com.cn:

- Gowin FPGA Products Programming and Configuration User Guide
- GW1N series FPGA Products Data Sheet
- GW1NR series FPGA Products Data Sheet

# 1.4 Abbreviation and Terminology

The abbreviations and terminologies used in this manual are as shown in Table 1-1 below.

**Table 1-1 Abbreviations and Terminologies**

| Abbreviation and Terminology | Full Name | Meaning |
|---|---|---|
| LUT | Look-up Table | Look-up Table |
| FPGA | Field Programmable Gate Array | Field Programmable Gate Array |
| SDRAM | Synchronous Dynamic Random Access Memory | Synchronous Dynamic RAM |
| PLL | Phase-locked Loop | PLL |
| DSP | Digital Signal Processing | Digital Signal Processing |
| JTAG | Joint Test Action Group | Joint Test Action Group |
| GPIO | General Purpose Input Output | General Purpose Input Output |
| SPI | Serial Peripheral Interface | Serial Peripheral Interface |
| SRAM | Static Random Access Memory | Static Random Access Memory |
| IEEE | Institute of Electrical and Electronics Engineers | Institute of Electrical and Electronics Engineers |
| TBD | To Be Determined | To Be Determined |
| ID | Identification | Identification |
| CRC | Cyclic Redundancy Check | Cyclic Redundancy Check |

# 1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

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# 2 Introduction

GW1N(R) series FPGA products are the first generation products of(LittleBee®)® family, with the features like low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage. GW1N series FPGA products contains GW1N-1, GW1N-2, GW1N-4, GW1N-6, and GW1N-9. The corresponding number of basic cell LUT4(4 Look-up Table) is 1K, 2K, 4K, 6K, and 9K , and the Max. user I/O is 272. Other than LUT4, GW1N series FPGA products support PLL, Block SRAM, User Flash, and I/O resources with multiple level standards. GW1N-2, GW1N-4, GW1N-6, and GW1N-9 support DSP. The basic cell LUT4 in GW1N-6 and GW1N-9 can be configured as S-SRAM.

The devices with same specifications in GW1NR series FPGA products and GW1N series FPGA products have same internal resources (LUT4, PLL, Memories, DSP, etc.). Based on GW1N series, GW1NR series FPGA products integrates SDRAM with the capacity 1024K x 16bit x 4bank. For the programming and configuration features, GW1N and GW1NR series FPGA products are the same.

The user flash used in GW1N-1 is from Huali; the user flash used in GW1N(R) series is from TSMC.

GW1N-1 device support lower voltage (LV) of 1.2V core voltage; the other GW1N(R) series FPGA products support both lower voltage (LV) and upper voltage(UV). LV supports 1.2V core voltage to meet users low power demands. $V_{CCO}$ supplied with IO Bank can be set as 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V according to requirements. UV devices support 1.8V, 2.5V, and 3.3V, and linear voltage regulator is integrated to facilitate single power supply.

**Caution!**

**Auxiliary voltage $V_{CCX}$only support 2.5V and 3.3V for both UV and LV, and VCCX must be greater than or equal to VCCO.**

GW1N(R) series FPGA products support three speed grade levels: -4, -5, and -6. "-6" means fast devices.

**Note!**

Apart from the different core voltages, the internal resources and pins of LV and UV devices are fully compatible.

# 3 Programming Configuration Notes

Besides JTAG, GW1N(R) series FPGA products also support GOWINSEMI own configuration mode GowinCONFIG. GowinCONFIG configuration modes supported for each device depends on device model and package. All the devices support JTAG and AUTO BOOT. Up to 6 configuration modes can be supported.

The features of GW1N(R) series FPGA Products Programming and Configuration are as follows:

- Instant start – millisecond
- Flexible configuration modes
- High security
- High capacity flash memory

**Note!**

- For details about configuration pins, pins multiplexing, and pins functions and application, please refer to *Gowin FPGA Programmign and Configuration User Guide* > *3 Configuration Pins Introduction*.
- For the configuration modes, power supply voltage, and other configuration notes of GW1NR series FPGA products, please refer to 3.1Configuration Modes Supported and 3.2Power Supply Voltage.

# 3.1 Configuration Modes Supported

Table 3-1 lists the configuration modes supported by GW1N(R) series FPGA products.

**Table 3-1 Configuration Mode**

| Configuration | | MODE[2:0][1] | Instructions |
|---|---|---|---|
| JTAG | | XXX[2] | GW1N(R) series FPGA products are configured by hardware processor via JTAG interface. |
| GowinCONFIG | AUTO BOOT | 000 | GW1N series FPGA products are configured by reading data from built-in Flash |
| | SSPI | 001 | GW1N(R) series FPGA products are configured by hardware processor via SPI interface. |
| | MSPI | 010 | As Master, GW1N series FPGA products are configured by reading data from external Flash (or other device) through SPI interface[3]. |
| | DUAL BOOT[4] | 100 | Read from built-in Flash first, and read from external Flash if built-in Flash configuration fails |
| | SERIAL[5] | 101 | GW1N(R) series FPGA products are configured by hardware processor via DIN interface. |
| | CPU[5] | 111 | GW1N(R) series FPGA products are configured by hardware processor via DBUS interface. |

**Note!**

- [1] For some of the devices packages, all the mode pins are not bonded out. The unbound mode pins are grounded;
- [2] JTAG configuration MODE is independent of MODE pins input value;
- [3] SPI interfaces of SSPI and MSPI mode are independent of each other;
- [4] GW1N(R)-2 and GW1N(R)-4 do not support DUAL BOOT now; GW1N(R)-6 and GW1N(R)-9 support DUAL BOOT with MODE value 100 and mode which start first from external Flash, and the MODE pins value is 110.
- [5] CPU configuration mode and SERIAL configuration mode share SCLK, WE_N and CLKHOLD_N; the data bus pins of CPU configuration mode share pins with MSPI and SSPI configuration modes.

# 3.2 Power Supply Voltage

GW1N(R) series FPGA products contains one power-on reset module, and the recommended power supply voltage is as shown in Table 3-2.

The device keeps reset state before the power supply conditions are met. When the conditions are met, the power-on reset circuit is released, allowing the device to begin its initialization process.

**Table 3-2 Recommended Power Supply Voltage**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $V_{CC}$ | LV: Core Power | 1.14V | 1.26V |
| | UV:Core Power | 1.71V | 3.465V |
| $V_{CCO}$ | I/O Bank Power | 1.14V | 3.6V |
| $V_{CCX}$ | Auxiliary Power | 2.3V | 3.465V |

# 4 Configuration Mode

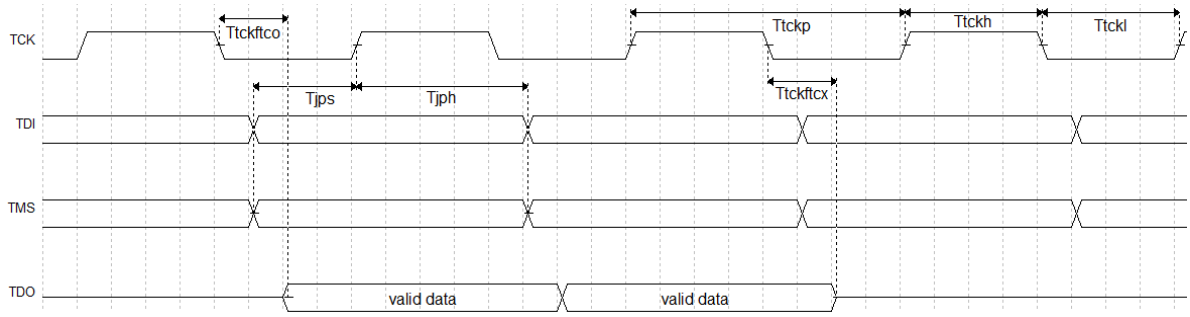
**Note!**

- This chapter mainly introduces the configuration modes timing diagrams and timing parameters supported by GW1N(R) series FPGA products.
- For the configuration modes pins definition and devices connection diagram, please refer to *Gowin FPGA Programming and Configuration User Guide*>*5 Configuration Modes Introduction*.

## 4.1 JTAG configuration

See Figure 4-1 for JTAG timing.

**Figure 4-1 JTAG Configuration timing**



See Table 4-1 for MSPI Timing Diagram.

**Table 4-1 JTAG Configuration Timing Parameters**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $T_{tckftco}$ | Time from TCK falling edge to output | - | 10ns |
| $T_{tckftcx}$ | Time from SCLK falling edge to high impedance | - | 10ns |
| $T_{tckp}$ | TCK clock period | 40ns | - |
| $T_{tckh}$ | TCK clock high time | 20ns | - |
| $T_{tckl}$ | TCK clock low time | 20ns | - |
| $T_{jps}$ | JTAG PORT setup time | 10ns | - |
| $T_{jph}$ | JTAG PORT hold time | 8ns | - |

# 4.2 AUTO BOOT

On chip Flash is configured via JTAG interface. After the configuration, RECONFIG_N is triggered by low pulse, or auto boot configuration starts after the power is cycled. Figure 4-2 and Figure 4-3 show the timing. For the auto boot configuration introduciton and auto boot configuration flow, please refer to *Gowin FPGA Prgrammign and Configuration User Guide*>*5 Configuration Modes Introduction*.

**Figure 4-2 GW1N Cycling Power Timing**

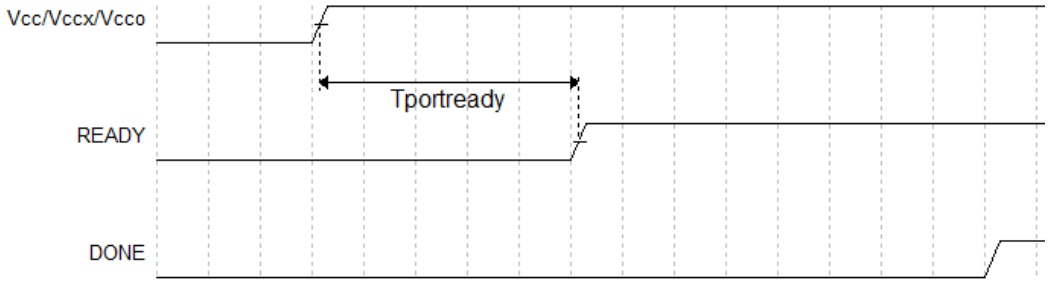



**Figure 4-3 GW1N RECONFIG_N Trigger Timing**

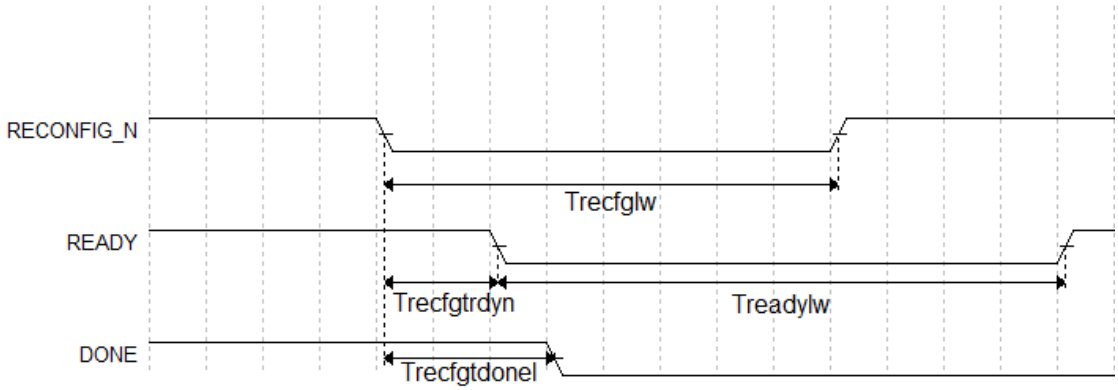


Figure Table 4-2 shows the timing.

**Table 4-2 Timing Parameters for Cycling Power and RECONFIG_N Trigger**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $T_{portready}$[1] | Time from application of $V_{CC}$, $V_{CCX}$ and $V_{CCO}$ to the rising edge of READY | 50μs | 200μs |
| $T_{recfglw}$ | RECONFIG_N low pulse width | 25ns | - |
| $T_{recfgtrdyn}$ | Time from RECONFIG_N falling edge to READY low | - | 70ns |
| $T_{readylw}$ | READY low pulse width | TBD | - |
| $T_{recfgtdonel}$ | Time from RECONFIG_N falling edge to READY low | - | 80ns |

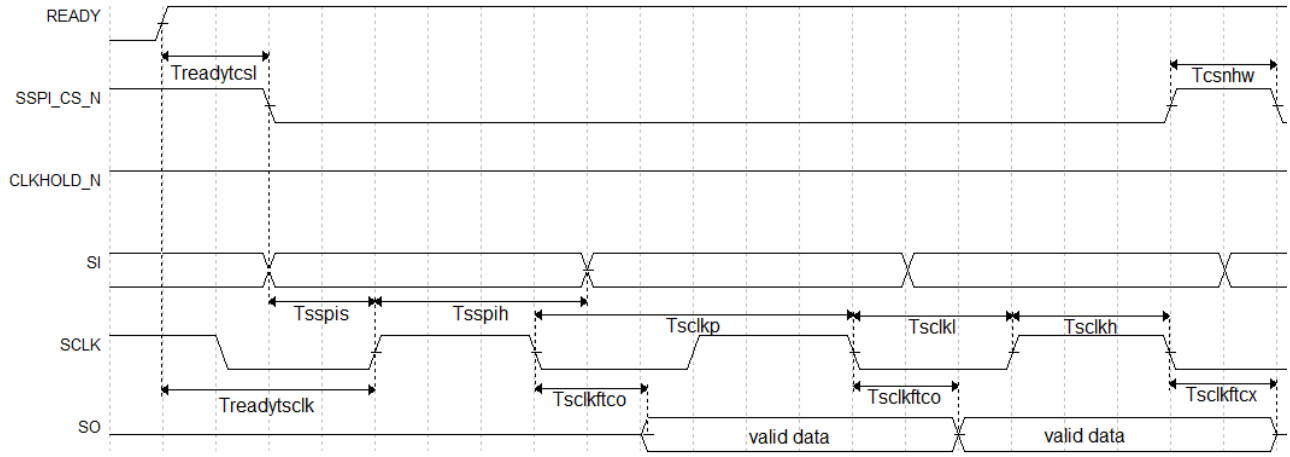
**Note!**

MODE0=0, the device power up waiting time is 200μs; MODE0=1, the device power up waiting time is 50μs.

# 4.3 SSPI

See Figure 4-4 for SSPI timing.

**Figure 4-4 JTAG Configuration timing**



See Table Table 4-3 for the timing parameters.

**Table 4-3 SSPI Configuration Timing Parameters**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $T_{sclkp}$ | SCLK clock period | 15ns | - |
| $T_{sclkh}$ | SCLK clock high time | 7.5ns | - |
| $T_{sclkl}$ | SCLK clock low time | 7.5ns | - |
| $T_{sspis}$ | SSPI PORT setup time | 2ns | - |
| $T_{sspih}$ | SSPI PORT hold time | 0ns | - |
| $T_{sclkftco}$ | Time from SCLK falling edge to output | - | 10ns |
| $T_{sclkftcx}$ | Time from SCLK falling edge to high impedance | - | 10ns |
| $T_{csnhw}$ | CSN high time | 25ns | - |
| $T_{readytcsl}$ | Time from READY rising edge to CSN low | TBD | |
| $T_{readytsclk}$ | Time from READY rising edge to first SCLK edge | TBD | - |

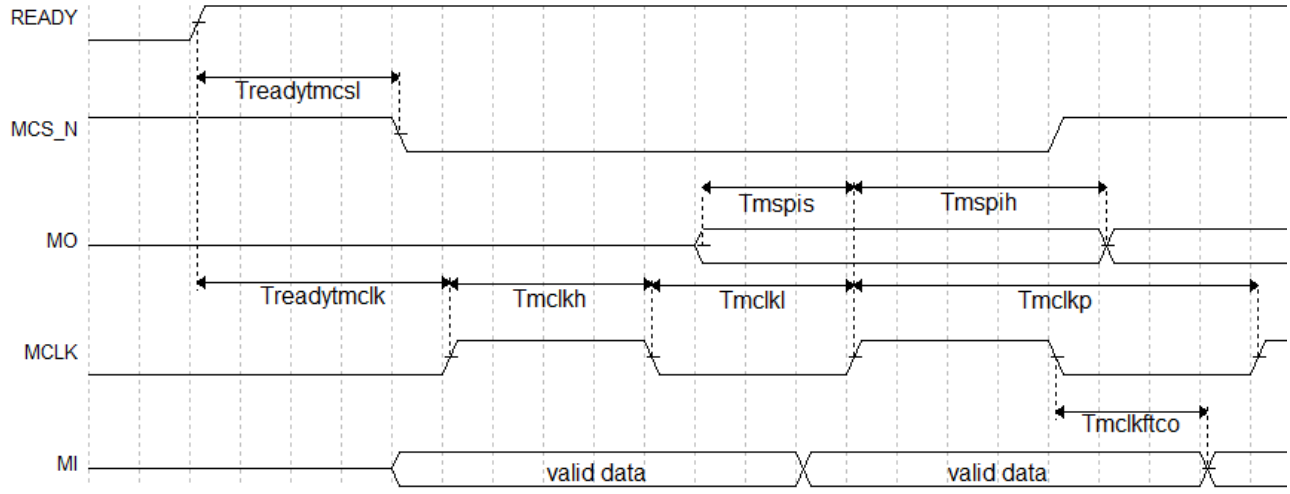
Other than the power requirements, the following conditions need to be met to use SSPI configuration mode:

- SSPI port enable
  Set RECONFIG_N as “NON-RECOVERY”.
- Initiate new program
  Power-on again or provide one low pulse ons programming pin RECONFIG_N.

# 4.4 MSPI

After MSPI writes the configuration data to the off chip Flash, power-on again or provide one low pulse on RECONFIG_N to trigger device configuration. See Figure 4-5 for MSPI timing.

**Figure 4-5 MSPI Download Timing**



See Table 4-4 for MSPI Timing parameters.

**Table 4-4 MSPI Configuration Timing Parameters**

| Name | Description | Min. | Max. |
|---|---|---|---|
| $T_{mclkp}$ | MCLK clock period | 15ns | - |
| $T_{mclkh}$ | MCLK clock high time | 7.5ns | - |
| $T_{mclkl}$ | MCLK clock low time | 7.5ns | - |
| $T_{mspis}$ | MSPI PORT setup time | 5ns | - |
| $T_{mspih}$ | MSPI PORT hold time | 1ns | - |
| $T_{mclkftco}$ | Time from MCLK falling edge to output | - | 10ns |
| $T_{readytmcsl}$ | Time from READY rising edge to MCS_N low | 100ns | 200ns |
| $T_{readytmclk}$ | Time from READY rising edge to first MCLK edge | 2.8μs | 4.4μs |

Other than the power requirements, the following conditions need to be met to use MSPI configuration mode:

- SSPI port enable
  Set RECONFIG_N as “NON-RECOVERY”.
- Initiate new program
  Power-on again or provide one low pulse for programming pin RECONFIG_N.

For the MSPI configuration modes features and devices supported, please refer to *Gowin FPGA Programming and Configuration User Guide* >*5 Configuration Modes Introduction*.

# 4.5 Dual-Boot

For the dual boot configuration introduction and dual boot configuration flow,please refer to *Gowin FPGA Programming and Configuration User Guide*>5 *Configuration Modes Introduction*.

# 4.6 CPU Mode

Other than the power requirements, the following conditions need to be met to use CPU configuration mode:

- SSPI port enables
  Set RECONFIG_N as “NON-RECOVERY”.
- Initiate new program
  Power-on again or provide one low pulse for programming pin RECONFIG_N.

# 4.7 SERIAL

Other than the power requirements, the following conditions need to be met to use CPU configuration mode:

- SERIAL port enables
  Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.
- Initiate new program
  Power-on again or provide one low pulse for programming pin RECONFIG_N.

# 5 Safety Precautions

Safety is a key factor for user to use FPGA. Combined with GW1N devices features, Gowin programmer offers a series of safety precautions, providing complete features for user bit stream.

Safety precautions consist of three stages:

- Before configuration, Gowin programmer checks the validity of bit stream;
- During configuration, GW1N device verifies the correctness of transmission data in real time;
- After configuration, GW1N device enters the working state, shielding any readback requests.

The details of the three stages are as follows:

## Before Configuration

Following steps describe how to use Gowin programmer to configure GowinFPGA.

1. Connect the device which needs to be configured;
2. Start Gowin programmer to scan and identify the connected FPGA device;
3. Select bit stream and configuration mode for the device configuration.

During the process above, Gowin programmer reads the connected device ID first, and then compares with the bit stream ID that the user selected. Configuration can proceed only when the two IDs are consistent, or the bit stream selected by user will be regarded as illegal data, resulting in configuration failure.

**Note!**

GW1N(R) series FPGA products have specific ID to distinguish with the other series products. The bit stream generated by Gowin Software contains ID verification directive, so users only need to select GW1N device when creating a new project.

## During Configuration

The device reads and verifies bit stream ID first, and configuration starts if verification passes. To prevent bit stream modifications or possible

transmission errors, GW1N devices adopts CRC to ensure bit stream is written in correctly. The specific process is as below.

Following each address segment of the bit stream, CRC is generated by Gowin Yunyuan software. GW1N device generates CRC in the process of receiving data and compares them with the check codes received. If CRC error is detected, the data after error will be ignored. The indicator "DONE" will not light up after configuration, and the CRC error message will be displayed on Gowin programmer interface.

### After Configuration

After configuration, the device bit stream is loaded to SRAM or on chip Flash according to user mode selection.

- If it is loaded to SRAM, Gowin Yunyuan software sets security bit automatically in the process of bit stream generation. No user can read SRAMs.
- If it is loaded to on chip flash, Flash is configured as auto boot mode after Flash configuration is complete. Any reading requests will be prohibited.

Besides that, the auto boot mode of GW1N(R) series FPGA products requires no connection to the external download interface, which helps greatly reduces the risk of data interception and provides user higher security. DUAL BOOT provides a selection for users to write backup bit streams to off chip Flash according to requirements.

**Note!**

GOWINSEMI takes no responsibility to the security of off chip Flash.

# 6On Chip Flash Programming

GW1N(R) series FPGA products consists of two kinds: GW1N-1 with Huali Flash embedded; the other GW1N(R) devices with TSMC Flash embedded.

On chip Flash is divided as three areas, which are data storage area, device information storage area(chip ID, pattern, etc.), and user Flash area (user storage) respectively. Users have read and write and erasure permissions for User Flash only in consideration of device information and internal data security.

## 6.1 Huali Flash（GW1N-1）

GW1N series FPGA products support User Flash with 12 Kbytes (48 page x 256 Bytes). The features are as follows:

- 100,000 write cycles
- Greater than10 years Data Retention at +85℃
- Selectable 8/16/32 bits data-in and data-out
- Page size: 256 Bytes
- 3μA standby current
- Page Write Time: 8.2ms

## 6.2 TSMC Flash（GW1N-2/4/6/9,GW1NR-4）

The user flash features of GW1N(R) series FPGA products are as follows:

- 10,000 write cycles
- Greater than10 years Data Retention at +85℃
- Page Erase Capability: 2,048 bytes per page
- Fast Page Erasure/Word Programming Operation
- Working speed:≤ 25ns
- Word Programming Time:≤16μs
- Page Erasure Time:≤120ms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