Gowin LVDS7:1 RX LVDS4:1 TX Reference Design
User Guide

TN656-1.00E,12/20/2017

Disclaimer

Revision History

Date	Version	Description
12/20/2017	1.00E	Initial version.

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1 About This Guide

1.1 Purpose

This guide describes LVDS7:1 RX LVDS4:1 TX Reference Design. LVDS7:1 RX LVDS4:1 TX Reference Design mainly documents its functions and features, ports and timing etc., which helps users to quickly understand features and usage of Gowin LVDS71 RX LVDS41 TX Reference Design.

1.2 Supported Products

The information in the guide applies to the following products:

GW2A series FPGA products: GW2A-18

1.3 Related Documents

The latest user guides are available on our Website. Refer to the related documents via http://www.gowinsemi.com.cn:

GW2A series FPGA Products Data Sheet

1.4 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name	Meaning
FPGA	Field Programmable Gate Array	Field Programmable Gate Array
LVDS	Low-Voltage Differential Signaling	Low-Voltage Differential Signaling
I/O	Input/Output	Input/Output
PLL	Phase Locked Loop	PLL

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

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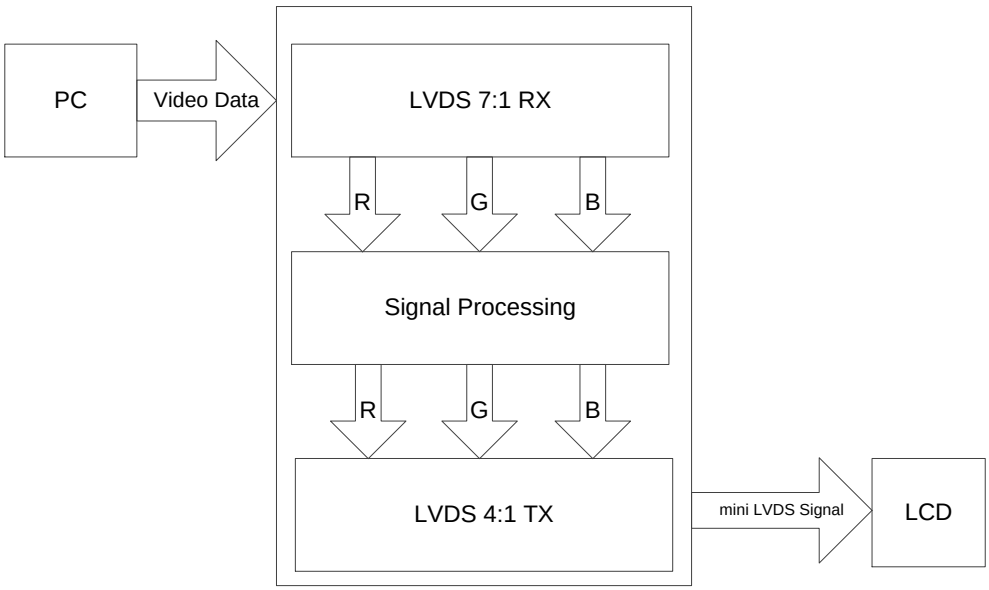
2 Overview

2.1 Introduction

LVDS7:1 RX LVDS4:1 TX Reference Design is mainly applied to TCON board, which can convert LVDS video signals to LVDS data signals used for the data driving circuit to realize that 1080P MB drivers 4 k2k LCD screen.

The data port of LVDS7:1 RX LVDS4:1 TX Reference Design converts the video image data received from PC to the low speed video signal via VDS7:1 RX module using a LVDS I/O, and converts the low speed video signal to the RGB signal needed for LCD screen using the signal processing module, then converts the RGB signal to mini-LVDS signal and sends it to the LVDS RX chip. The structure diagram is shown as Figure 2-1.

Figure 2-1 Structure Diagram of LVDS7:1 RX LVDS4:1 TX Reference Design



3 Features and Performances

3.1 Key Features

- Comply with LVDS and mini LVDS port standard;
- Adoptlow-voltage differential signaling;
- Support data transmission with high speed, low noise, long distance, and high accuracy.

3.2 Max. Frequency

The timing interface rate can be up to 800Mbps.

3.3 Resource Utilization

LVDS7:1 RX LVDS4:1 TX Reference Design can be realized via Verilog which is applied to GW2A-18-LQFP144 FPGA. Resource utilization is as shown in Table 1.

Table 1 Resource Utilization

Package Information	Speed Grade	Name	Resource Utilization	Remarks
GW2A-18-LQFP144	-6	LUT	1452	contains word alignment and bit alignment modules
		ALU	61	
		PLL	2	
		CLKDIV	5	
		REG	790	

4 Functional Description

4.1 Functions

LVDS7:1 RX LVDS4:1 TX Reference Design includes three modules:

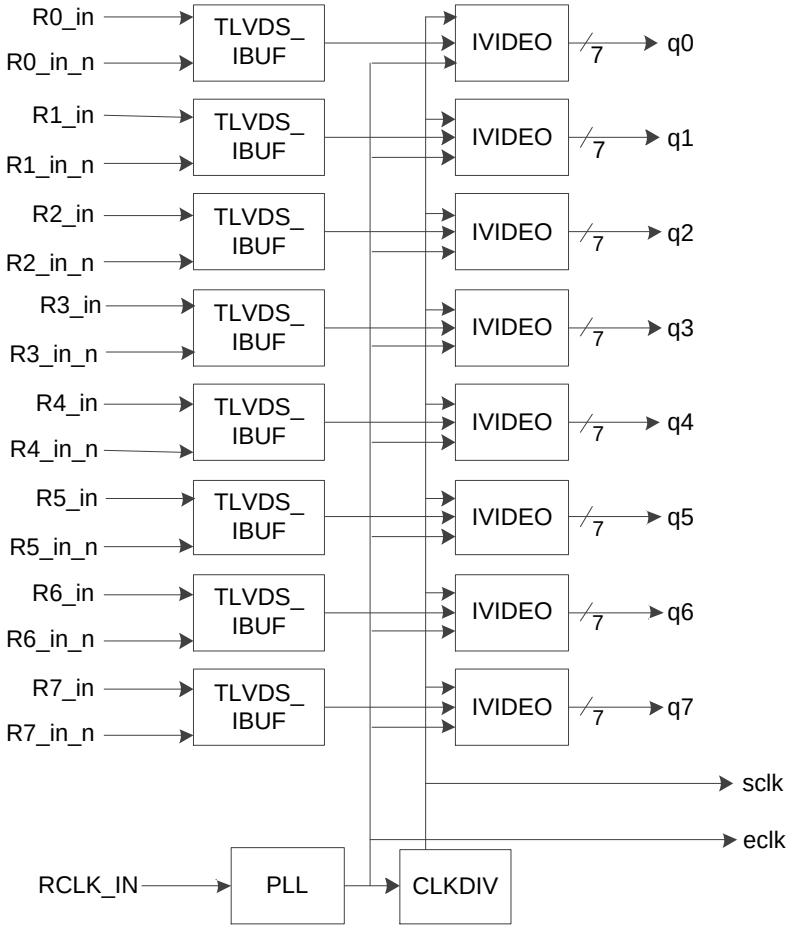
- LVDS 7:1 RX module
- DSP
- LVDS 4:1 TX module

LVDS 7:1 RX module receives the video signal from the PC (or DVD, etc.) and convert it to 7:1 source sync signal; Signal processing module processes and converts the data signal to RGB signal needed for the LCD; LVDS 4:1 TX module converts the RGB signal to a mini LVDS signal that can drive the LCD screen.

4.2 LVDS 7:1 RX Module

LVDS 7:1 RX module receives video signal using the LVDS differential interface, parallelly processes the differential signal and convert it to 7:1 low speed data signal; generates 3.5 times and 1.75 times clocks based on the input clock signal using PLL and CLKDIV, handles the wobble and deflection of the clock using the alignment module. Figure 4-1 shows the function diagram of LVDS 7:1 RX module.

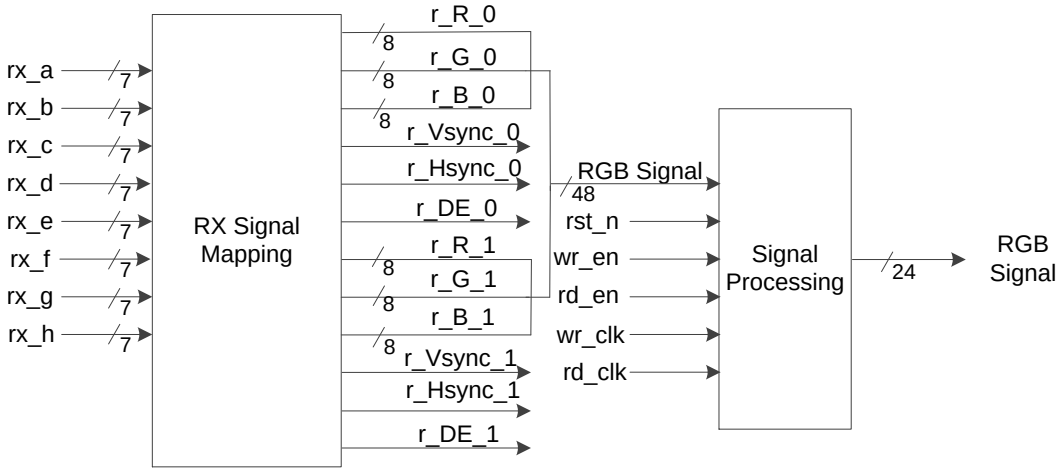
Figure 4-1 Function Diagram of Lvds 7:1 Rx Module



4.3 DSP

DSP supports signal mapping processing for the data signal transmitted by LVDS 7:1 RX module to receive two-channel RGB signals, line/field signal and enable control signal synchronously transmitting with the pixel clock. Four-channel 24-bit RGB signals will be got by adjusting the two-channel 8-bit RGB signals. Figure 4-2 shows the function diagram of one 24-bit RGB signal conversion.

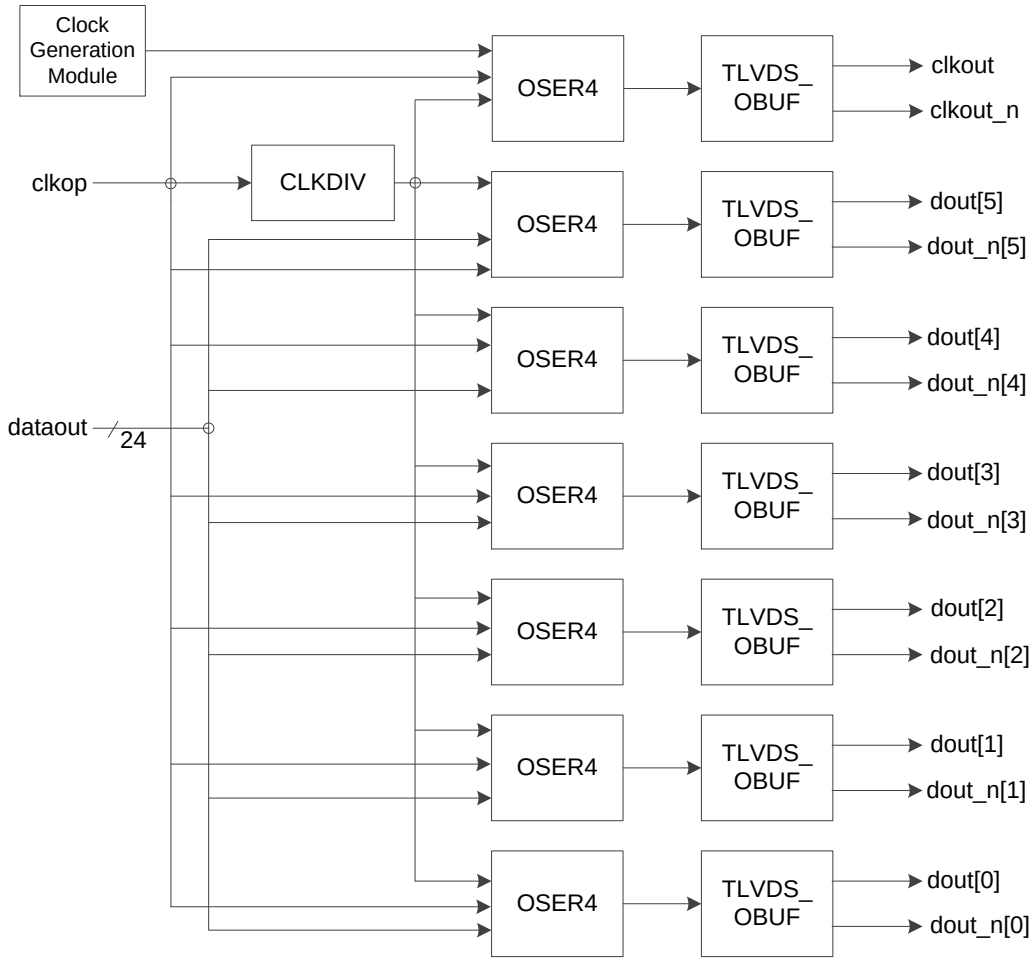
Figure 4-2 Function Diagram Of 24-Bit RGB Signal Conversion



4.4 LVDS 4:1 TX Module

Based on the sampling clock of clock signal outputted by the LVDS 7:1 RX module, LVDS 4:1 TX module converts 24-bit data signal outputted by the signal processing module to 6-bit mini LVDS signal and generates the clock signal needed for driving the LCD screen. Function diagram of one LVDS 4:1 RX module is as shown in Figure 4-3.

Figure 4-3 Function Diagram of LVDS 7:1 TX Module

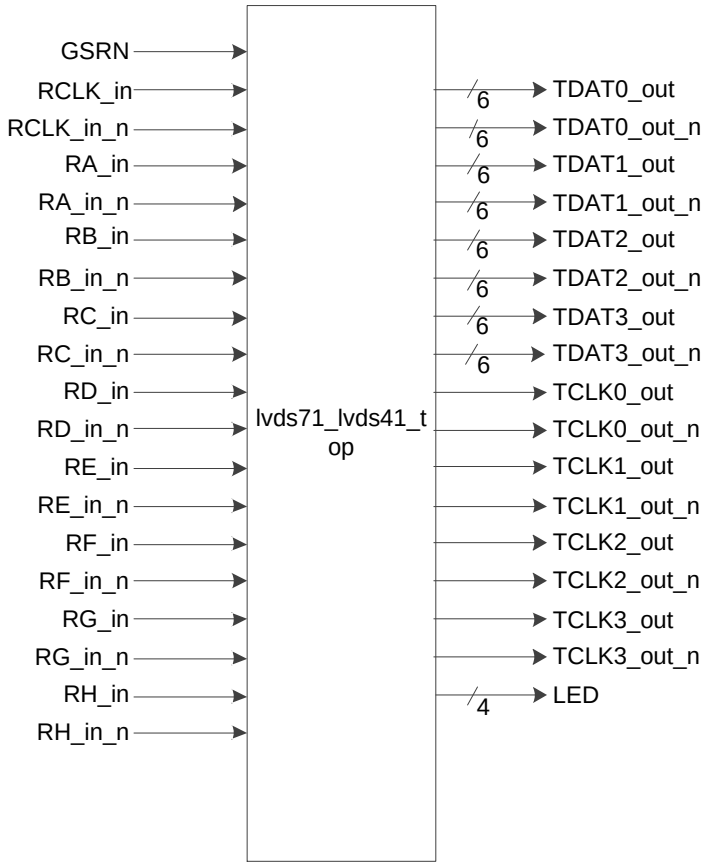


5 Ports Description

5.1 Ports Diagram

Ports Diagram of LVDS7:1 RX LVDS4:1 TX Reference Design is shown in Figure 5-1.

Figure 5-1 LVDS7:1 RX LVDS4:1 TX Reference Design Ports



5.2 Port Signal

Ports signal of LVDS7:1 RX LVDS4:1 TX Reference Design is shown in Table 51.

Table 51 LVDS7:1 RX LVDS4:1 TX Reference Design Port Signal

Port Name	Port Type	Description
GSRN	input	Reset signal
RCLK_in	input	Clock differential signal
RCLK_in_n	input	Clock differential signal
RA_in	input	Differential signal of data channel A
RA_in_n	input	Differential signal of data channel A
RB_in	input	Differential signal of data channel B
RB_in_n	input	Differential signal of data channel B
RC_in	input	Differential signal of data channel C
RC_in_n	input	Differential signal of data channel C
RD_in	input	Differential signal of data channel D
RD_in_n	input	Differential signal of data channel D
RE_in	input	Differential signal of data channel E
RE_in_n	input	Differential signal of data channel E
RF_in	input	Differential signal of data channel F
RF_in_n	input	Differential signal of data channel F
RG_in	input	Differential signal of data channel G
RG_in_n	input	Differential signal of data channel G
RH_in	input	Differential signal of data channel H
RH_in_n	input	Differential signal of data channel H
TCLK0_out	output	Synchronous clock source CLK0
TCLK0_out_n	output	Synchronous clock source CLK0
TCLK1_out	output	Synchronous clock source CLK1
TCLK1_out_n	output	Synchronous clock source CLK1
TCLK2_out	output	Synchronous clock source CLK2
TCLK2_out_n	output	Synchronous clock source CLK2

Port Name	Port Type	Description
TCLK3_out	output	Synchronous clock source CLK3
TCLK3_out_n	output	Synchronous clock source CLK3
TDAT0_out[5:0]	output	Output serial data at port TX of 0-channel
TDAT0_out_n[5:0]	output	Output serial data at port TX of 0-channel
TDAT1_out[5:0]	output	Output serial data at port TX of 1-channel
TDAT1_out_n[5:0]	output	Output serial data at port TX of 1-channel
TDAT2_out[5:0]	output	Output serial data at port TX of 2-channel
TDAT2_out_n[5:0]	output	Output serial data at port TX of 2-channel
TDAT3_out[5:0]	output	Output serial data at port TX of 3-channel
TDAT3_out_n[5:0]	output	Output serial data at port TX of 3-channel
LED[3:0]	output	Status/debug port

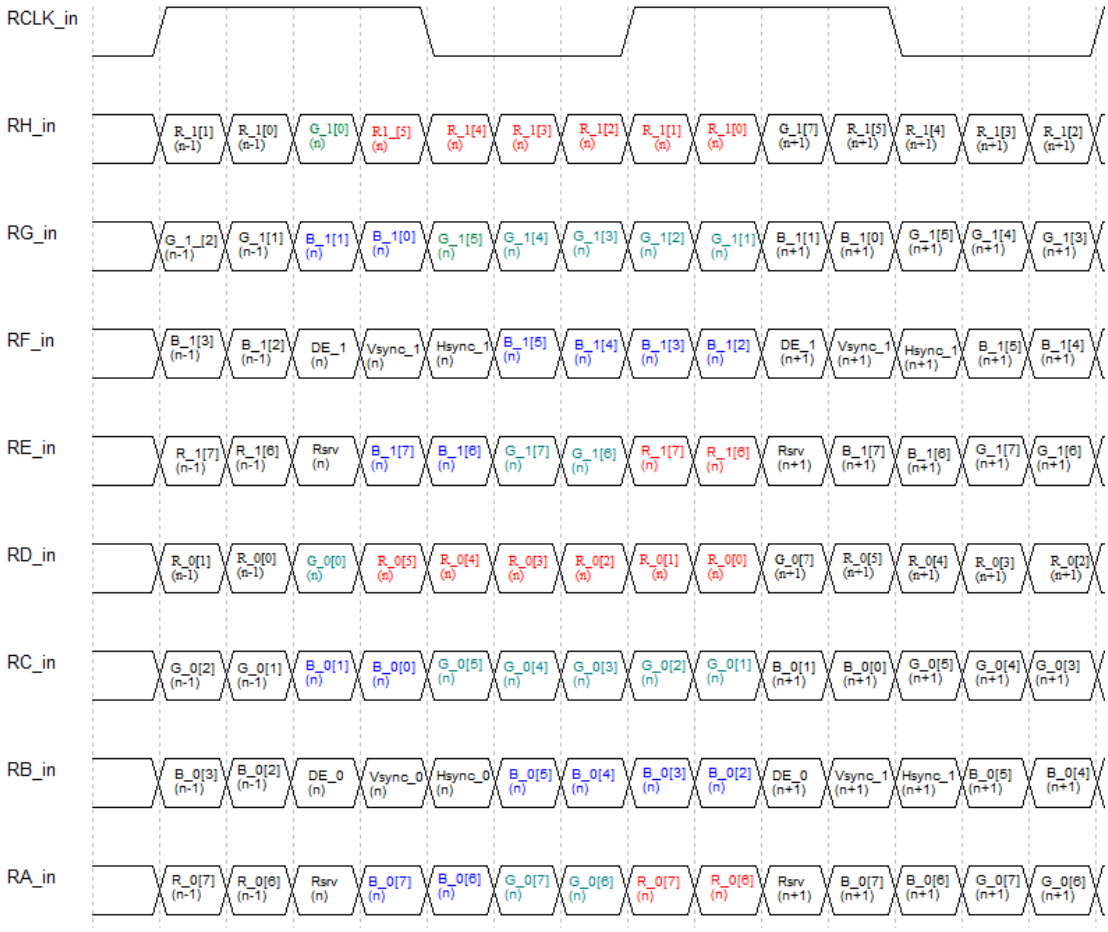
6 Timing Description

This chapter introduces the input signal timing of LVDS7:1 RX LVDS4:1 TX Reference Design.

6.1 Input Signal Timing

LVDS7:1 RX LVDS4:1 TX Reference Design is used for receiving video signals sent by PC, including one clock channel RCLK_in, 8 data channels (RA_in, RB_in, RC_in, RD_in, RE_in, RF_in, RG_in and RH_in), and a pair of differential data lines, which can transmit 7-bit data and signal timing, as shown in Figure 6-1.

Figure 6-1 Input signal timing of LVDS7:1 RX LVDS4:1 TX Reference Design

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